VLSI LABORATORY RECORD

R16

III / IV B.TECH (ECE) (R1632047)

II – SEMESTER

DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING

SIR C.R.REDDY COLLEGE OF ENGINEERING

ELURU – 534 007

SIR C.R.REDDY COLLEGE OF ENGINEERING, ELURU.

DEPARTMENT OF ELECTRONICS & COMMUNICATIONENGINEERING.

Certificate

This is to certify that this is the BONAFIED RECORD of the work done in …….Laboratory by Mr. / Ms……...

bearing Regd.No……of…….

B.Tech Course during 20 - 20 .

Total no.of Experiments Held: Total no.of Experiments done:

Lab In-charge Head of the Department

External Examiner

VLSI LABORATORY

Note: The students are required to design the schematic diagrams using CMOS logic and to draw the layout diagrams to perform the following experiments using 130nm technology with the Industry standard EDA Tools.

List of Experiments:

1. Design and Implementation of an Universal Gates
2. Design and Implementation of an Inverter
3. Design and Implementation of Full Adder
4. Design and Implementation of Full Subtractor
5. Design and Implementation of Decoder
6. Design and Implementation of RS-Latch
7. Design and Implementation of D-Latch
8. Design and Implementation asynchronous counter
9. Design and Implementation of static RAM cell
10. Design and Implementation of 8 bit DAC using R-2R latter network

Software Required:

1. Mentor Graphics Software / Equivalent Industry Standard Software.
2. Personal computer system with necessary software to run the programs and to implement.

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Name: Reg.No:

Name of the Laboratory: Code:

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S.No.	Name of the Experiment	Conducted on	Lab Performance (10)	Submitted on	Record (5)	Total (15)

S.No.	Name of the Experiment	Conducted on	Lab Performance (10)	Submitted on	Record (5)	Total (15)

Signature of the Lab in Charges	1. 2.	Average marks (15):

1. INVERTER

Date:

Aim: To generate schematic and layout for an inverter using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: Its name itself indicating that in performs inversion operation. It generates logic‘1’ as output for its logic‘0’ input and vise versa. Symbol of inverter is just as a buffer with a bubble mounted on its sharp end. It is used to perform logical operations.

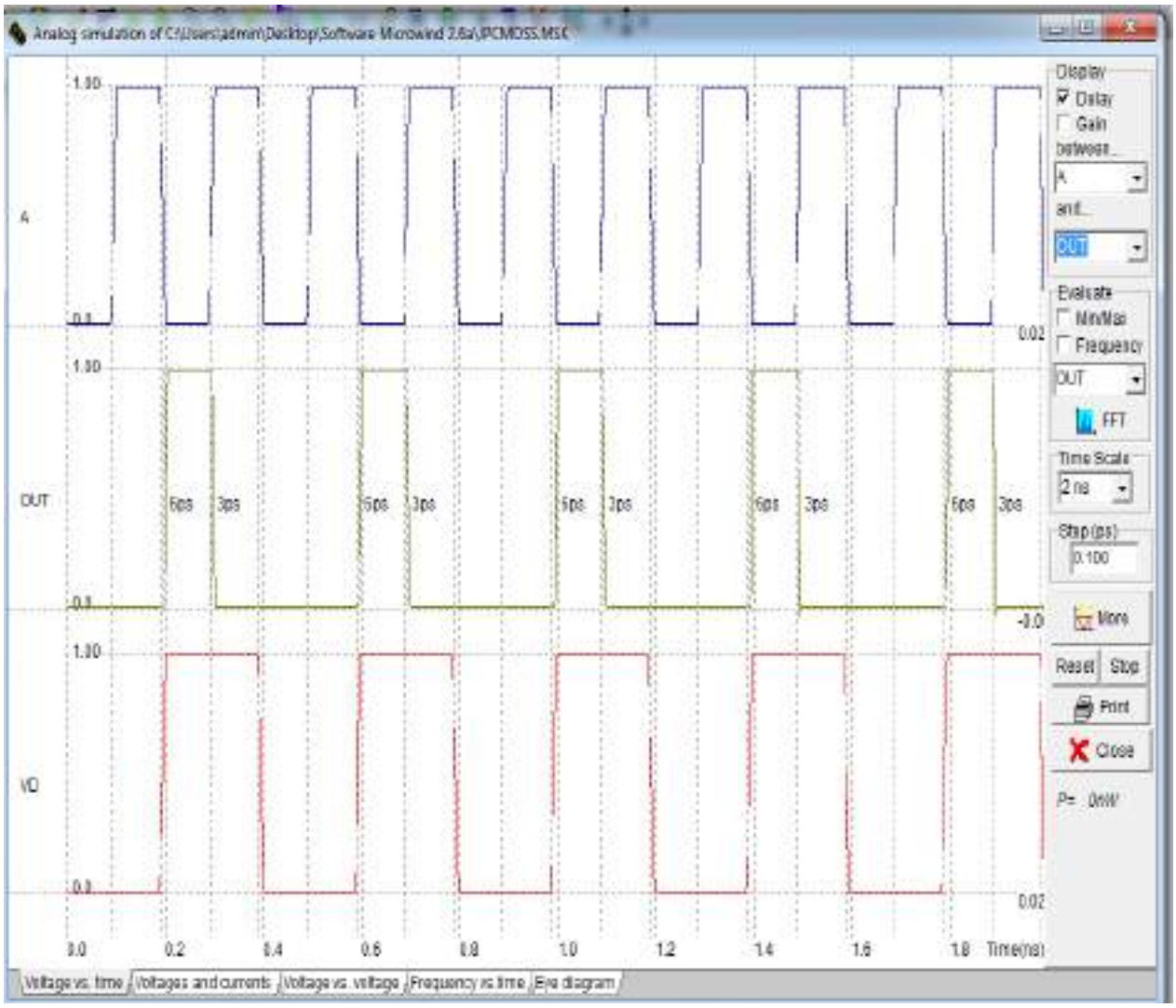
Truth table:

Input A	Output
0	1
1	0

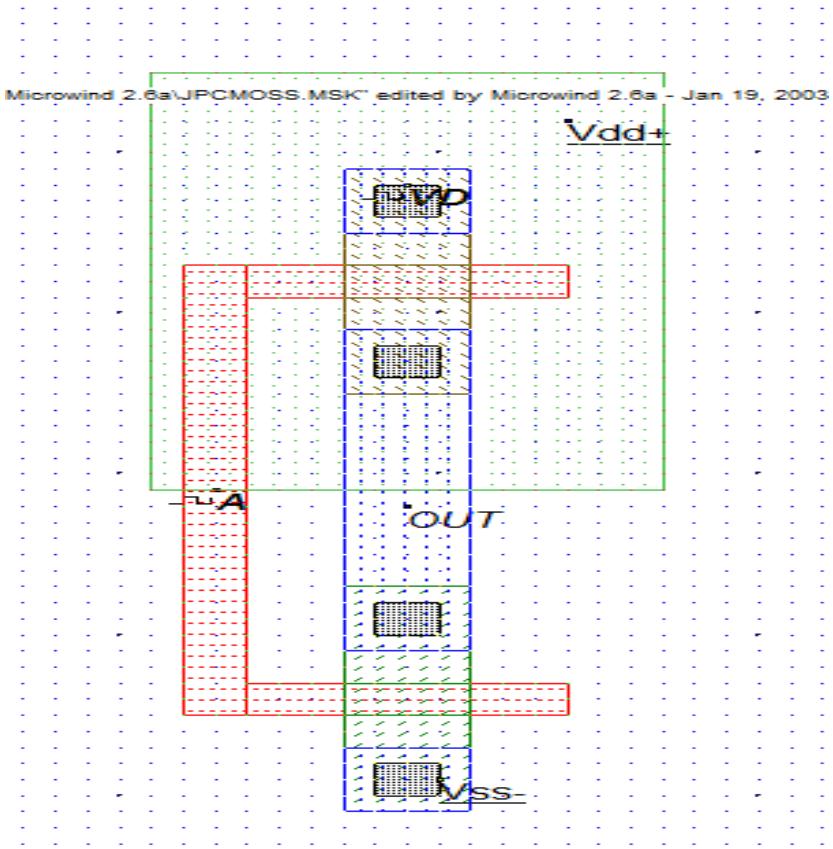
Schematic Diagram for Inverter:

Symbol for Inverter:

Waveforms for Inverter:



Layout for inverter:



Result: Hence simulated and verified the schematic and layout of inverter using DSCH & MICRO WIND tool.

2.1 NAND 2-INPUT GATE

Date:

Aim: To generate schematic and layout for an NAND Gate using DSCH & MICRO WIND tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND tool.

Theory: Nand gate is the logic component in this if any one of the input is '0' or low the output is high '1' otherwise if two inputs are equal to one then out put is low '0'. It is used to perform logical operations

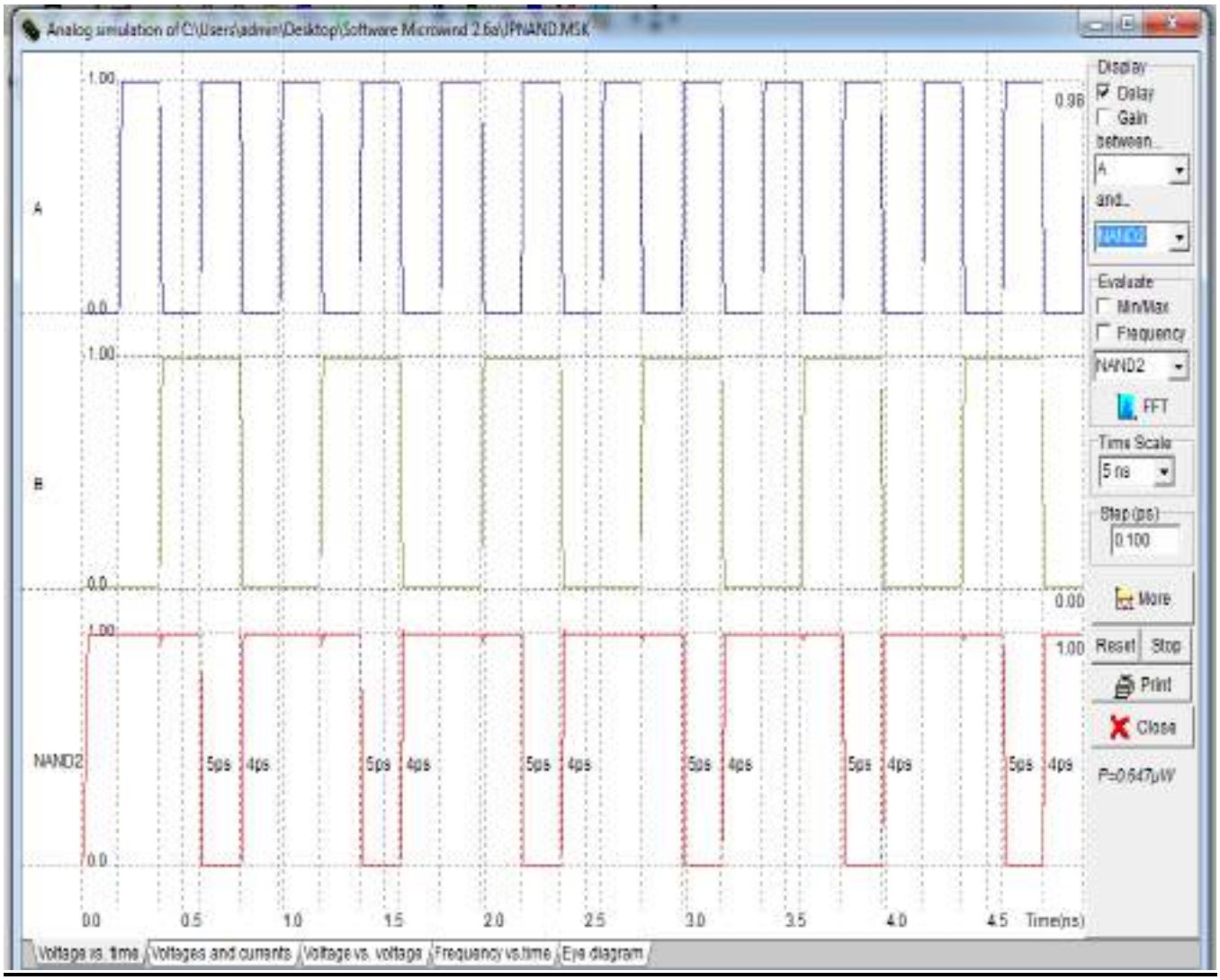
Truth table:

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

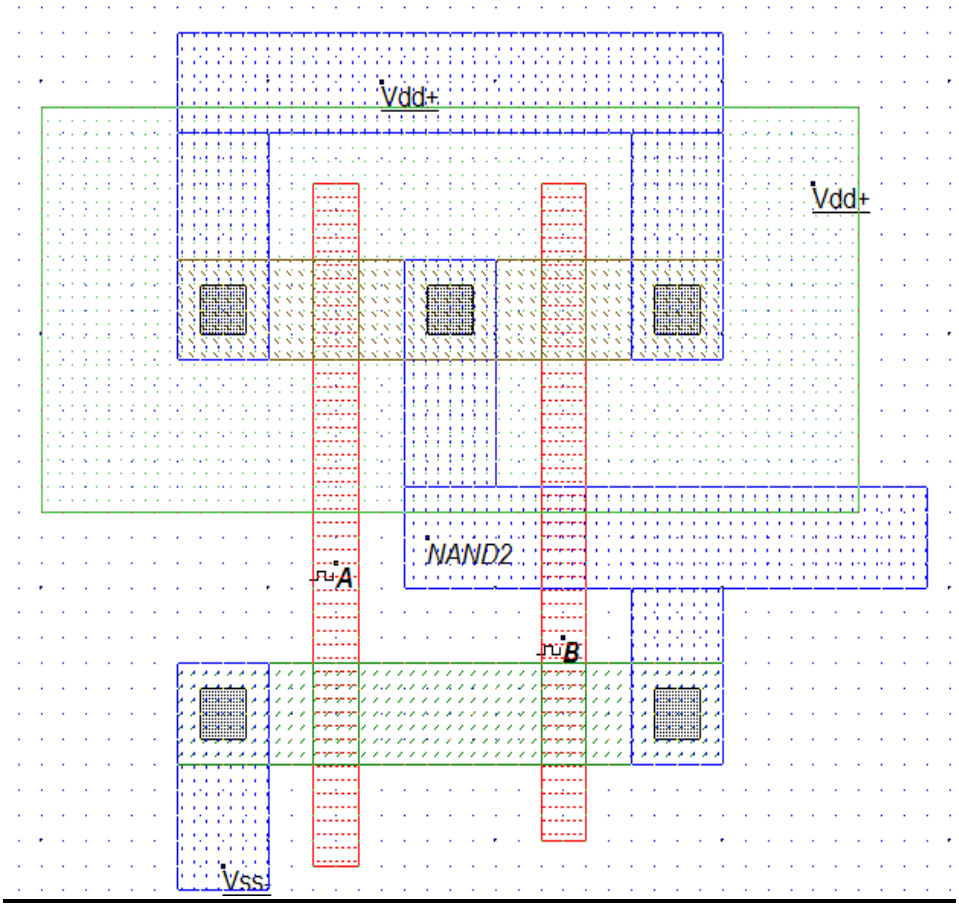
Schematic Diagram for NAND Gate:

Symbol for NAND Gate:

Waveforms for NAND Gate:



Layout for NAND Gate:



Result: Hence simulated and verified the schematic and layout of NAND Gate using DSCH & MICRO WIND tool.

2.2 NOR 2-INPUT GATE

Date:

Aim: To generate schematic and layout for NOR Gate using DSCH & MICRO WIND tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND tool.

Theory: NOR gate is the logic component in this if any one of the input is one the output is low '0' otherwise if two input are equal to '0' then the output is high '1'. It is used to perform logical operations

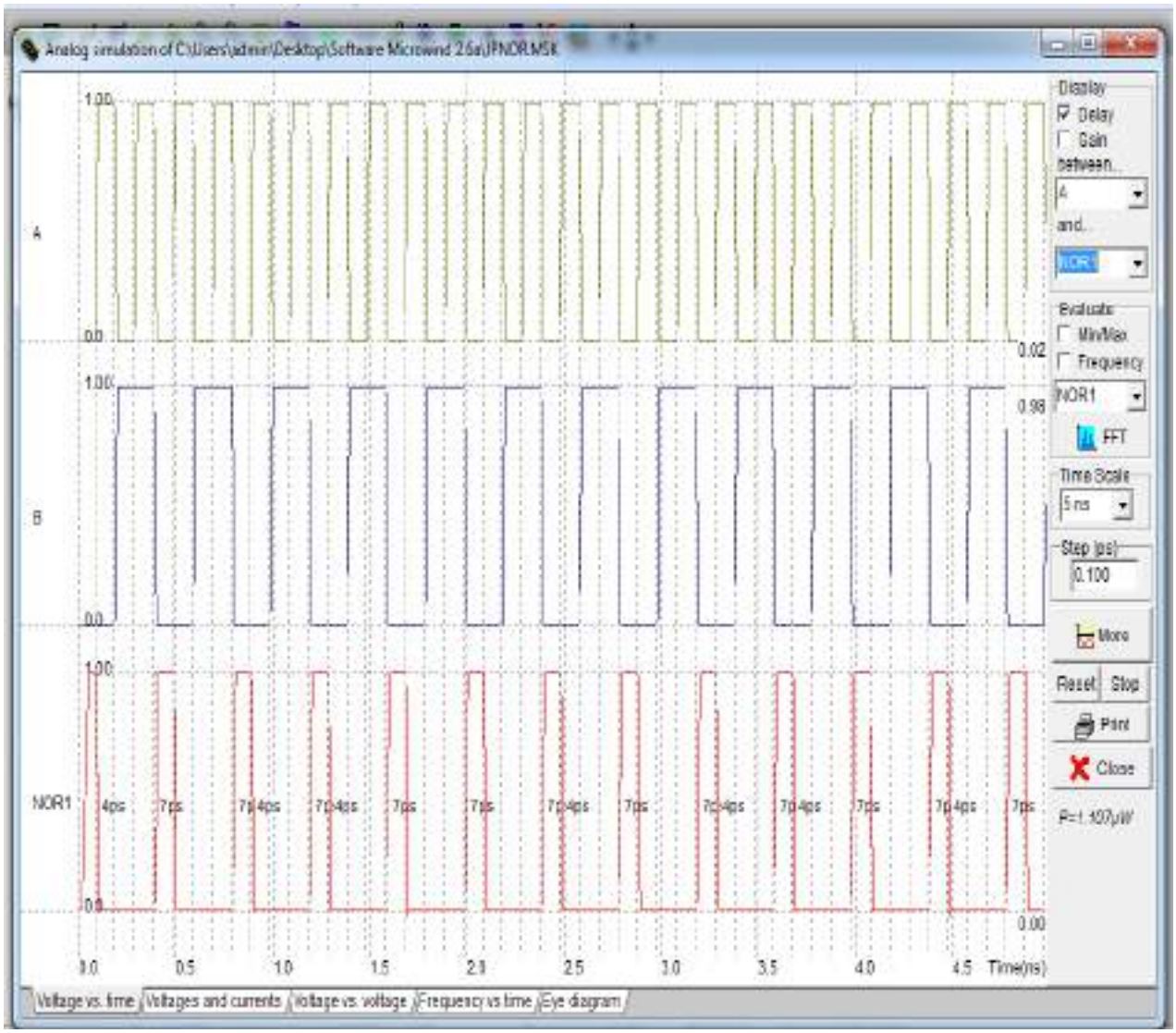
Truth Table:

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

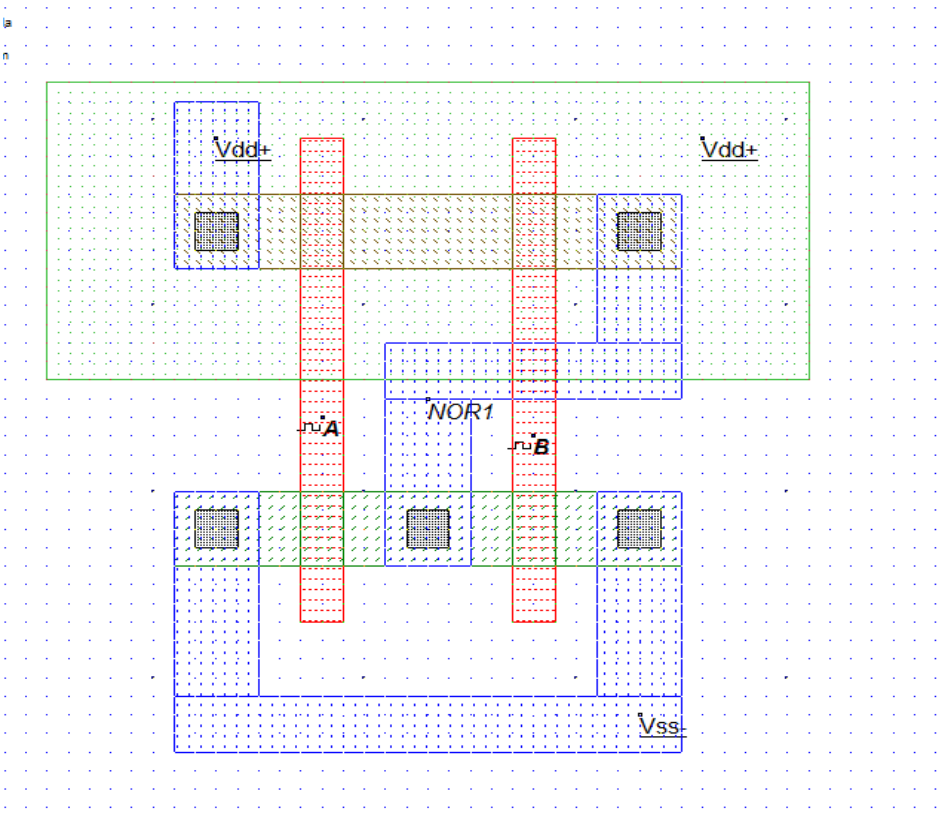
Schematic Diagram for NOR Gate:

Symbol for NOR Gate:

Waveforms for NOR Gate:



Layout for NOR



Result: Hence simulated and verified the schematic and layout of NOR Gate using DSCH & MICRO WIND Tool

3. FULL ADDER

Date:

Aim: To generate schematic for FULL ADDER using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: A logic circuit for the addition of three one bit binary numbers at a time is known as a full adder. The function of the circuit is to add three binary digits, producing both sum and carry. Hence the basic difference full adder and half adder is, full adder accepts an additional input that allows for handling input carriers. The carry is produced with an NAND Gate

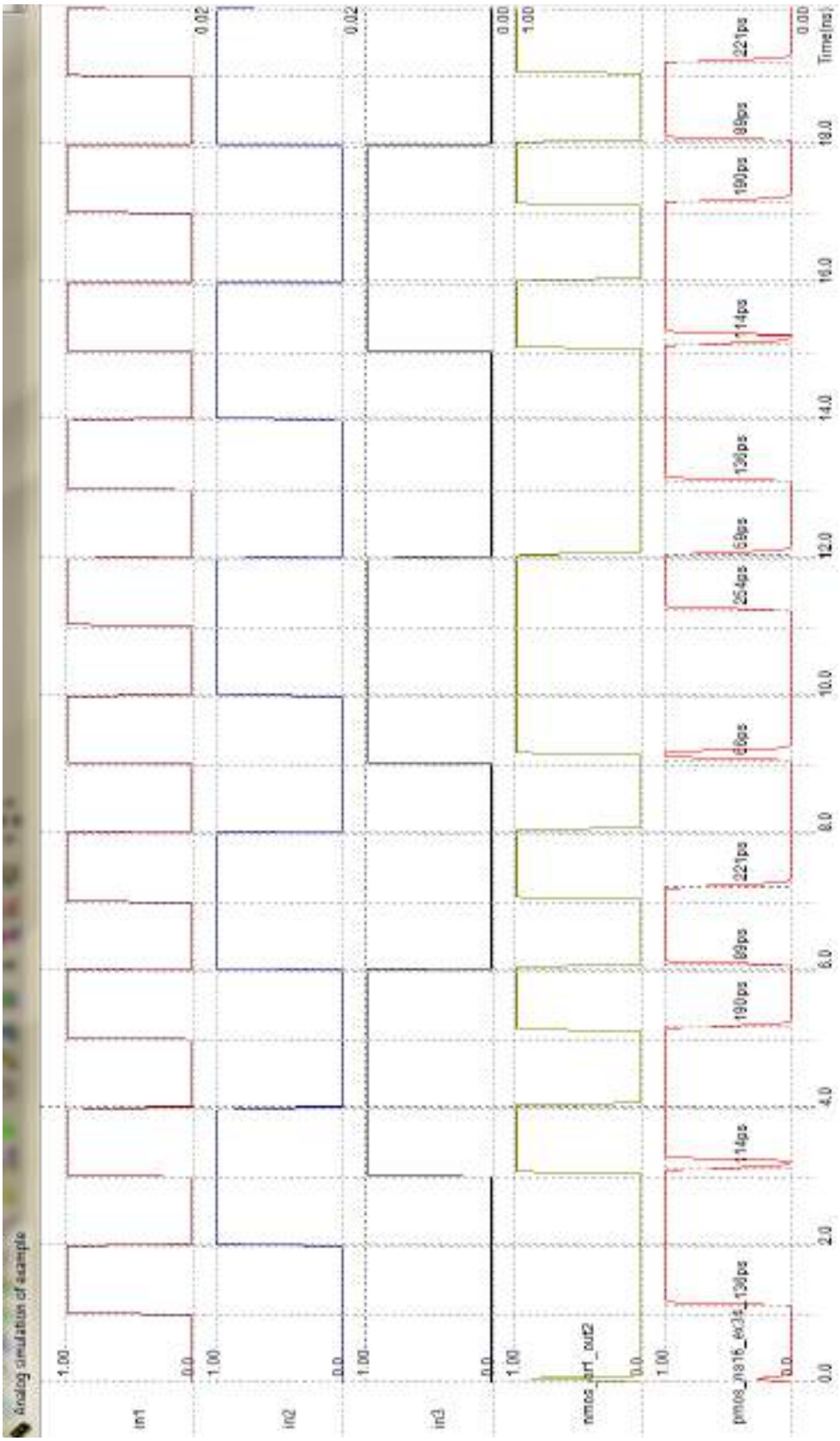
Truth Table:

Input A	Input B	Input C	sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

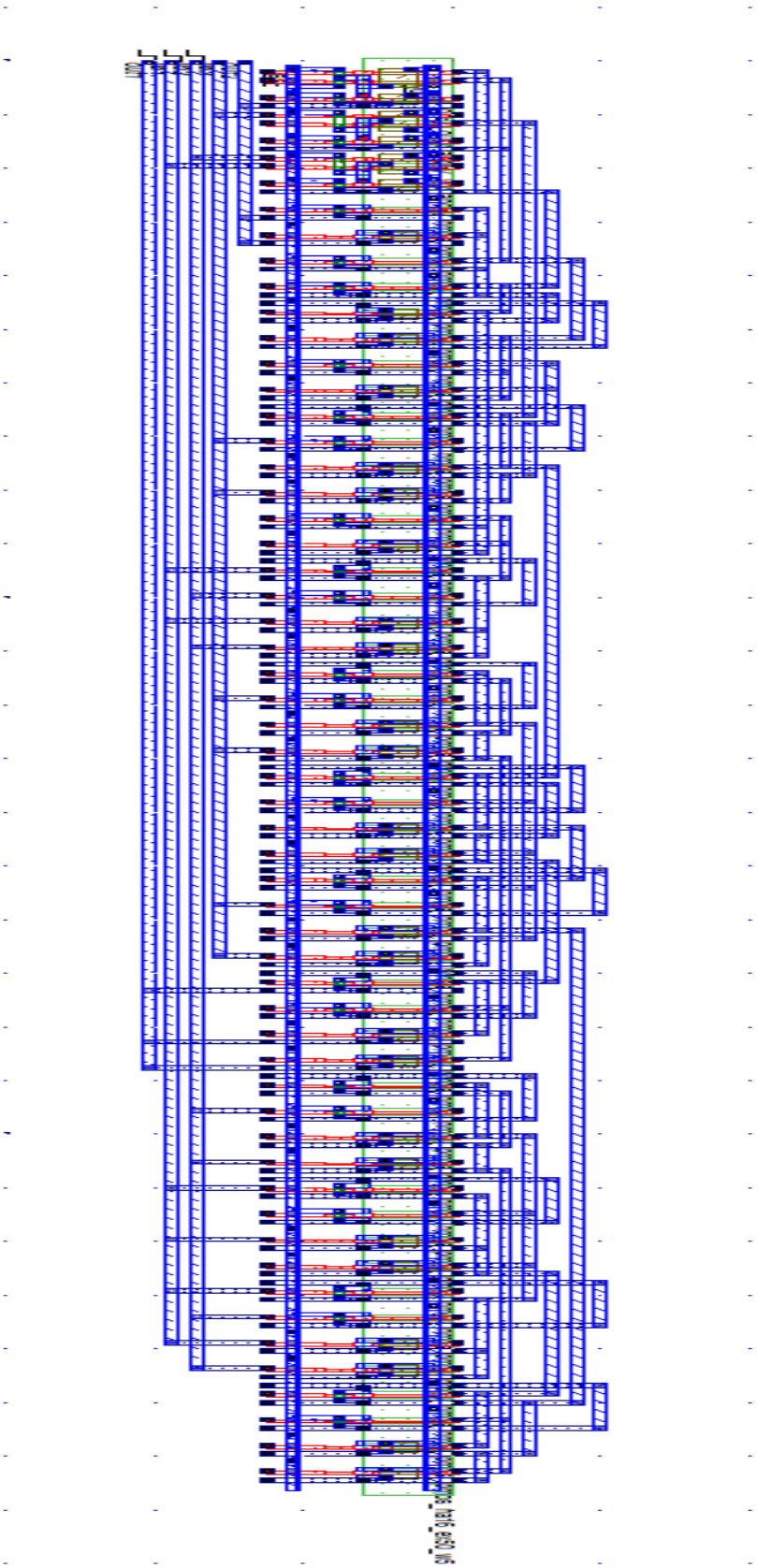
Schematic Diagram for Full Adder:

Symbol for Full Adder :

Waveforms for Full Adder:



Layout for FULL ADDER



Result: Hence simulated and verified the schematic of Full Adder using DSCH & MICRO WIND Tool.

4. FULL SUBTRACTOR

Date:

Aim: To generate schematic for a Full Subtractor using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: A logic circuit for the subtraction of three one bit binary numbers at a time is known as a full subtractor. The function of the circuit is to subtract three binary digits, producing both difference and borrow.

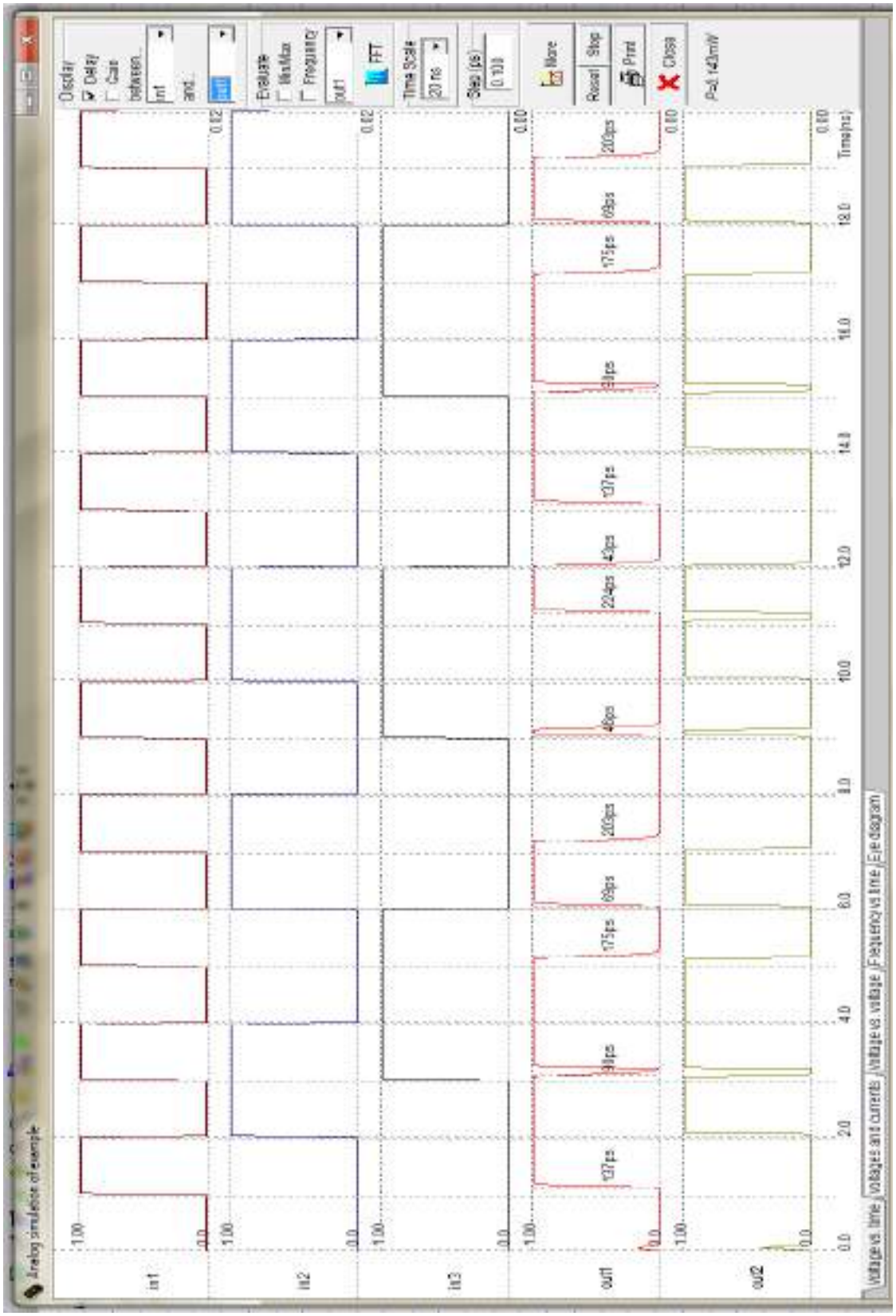
Truth Table:

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

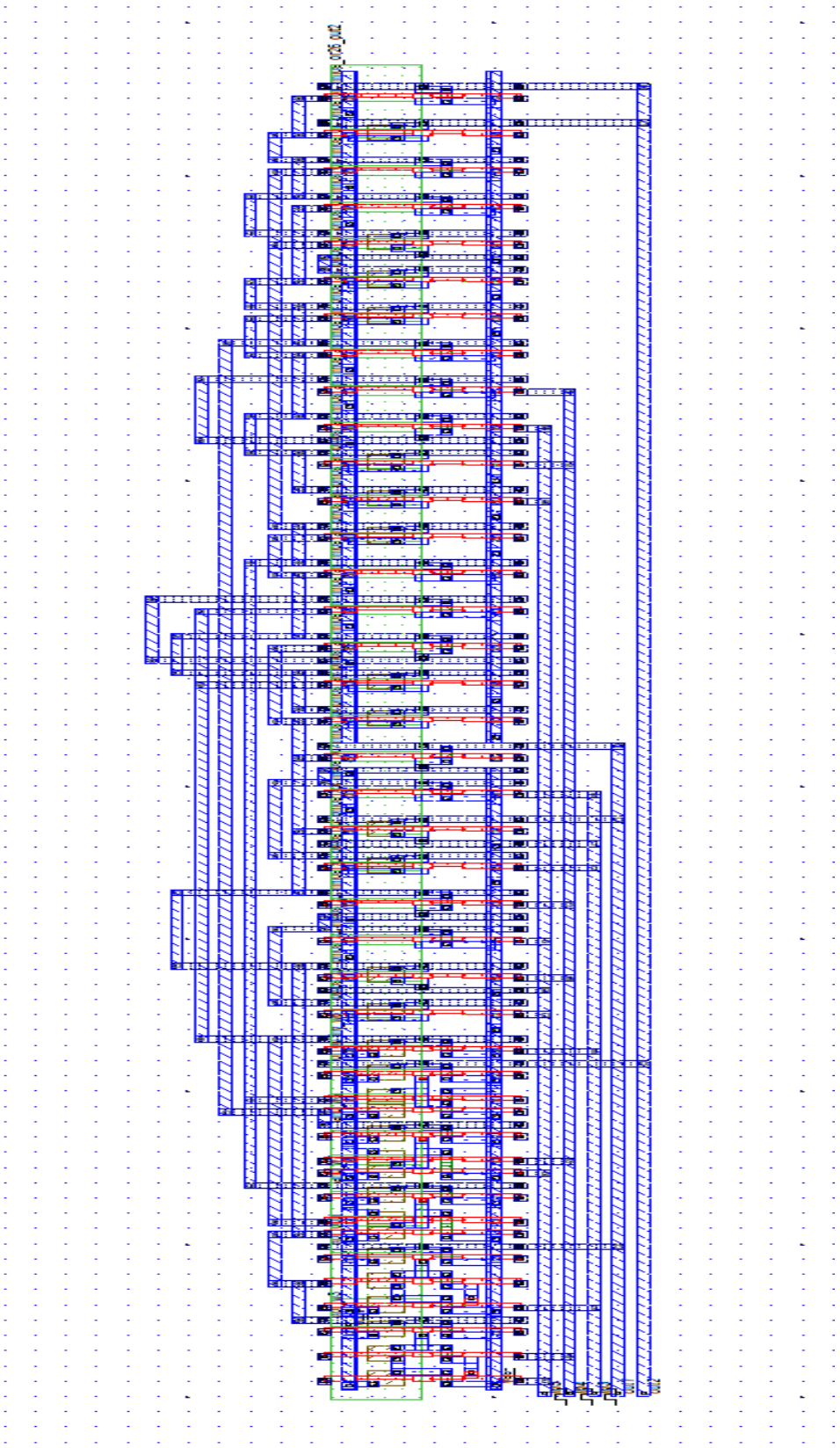
Schematic Diagram for Full Subtractor:

Symbol for Full Subtractor:

Waveforms for Full Subtractor:



Layout for FULL SUBTRACTOR:



Result: Hence simulated and verified the schematic of Full Subtractor using DSCH & MICRO WIND Tool.

5. Decoder

Date:

Aim: To generate schematic for decoder using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory:

A **decoder** is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. ... Sometimes an n-bit binary code is truncated to represent fewer than 2n values. A **decoder** is a combinational logic circuit which is used to change the code into a set of signals. It is the reverse process of an **encoder**. A **decoder** circuit takes multiple inputs and gives multiple outputs. A **decoder** circuit takes binary data of 'n' inputs into '2^n' unique output.

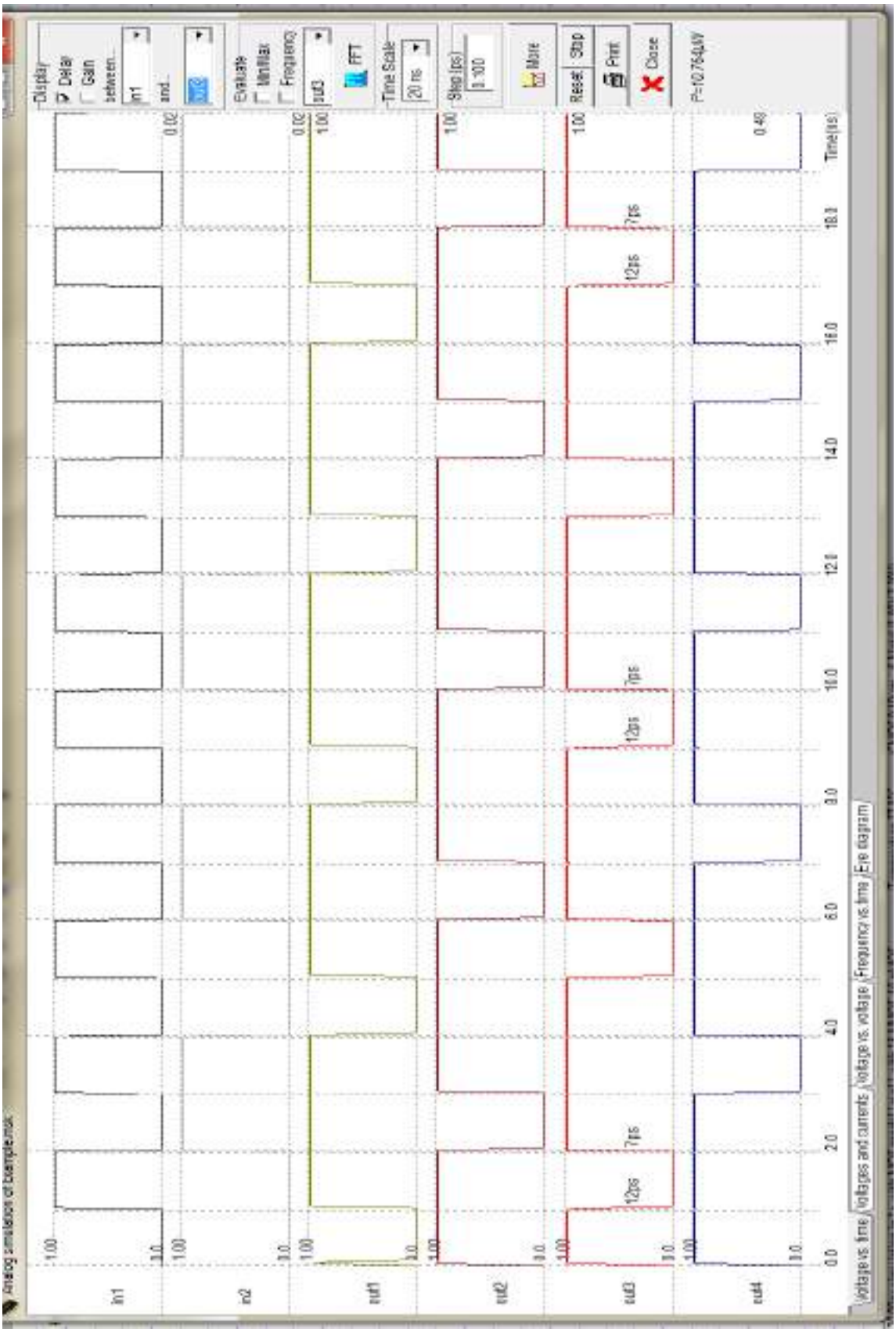
Truth Table:

Input		Enable	Output			
I1	I0	E	O3	O2	O1	O0
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

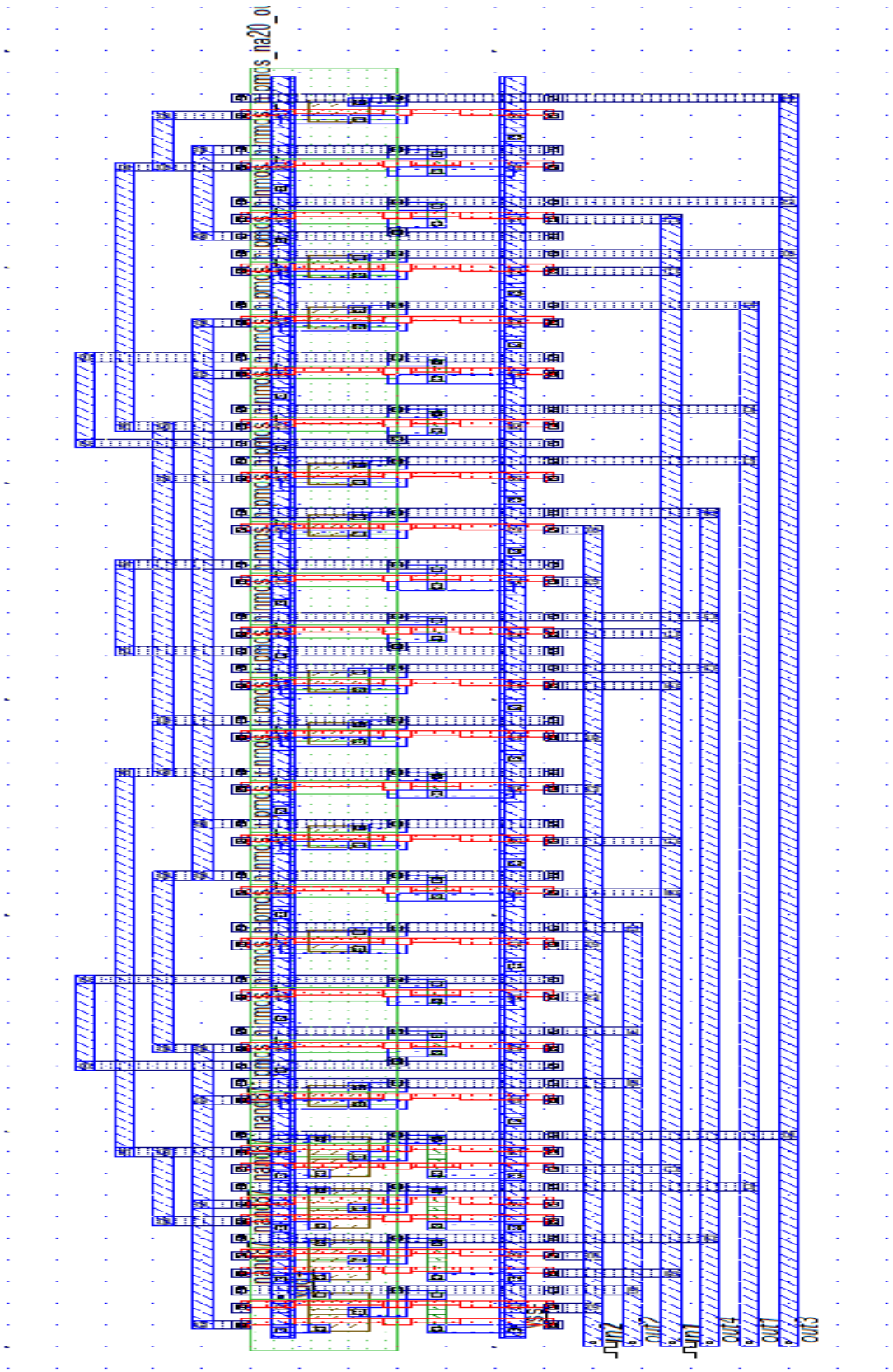
Schematic Diagram for decoder:

Symbol for decoder:

Waveforms for decoder:



Layout for DECODER:



Result: Hence simulated and verified the schematic of **decoder** using DSCH & MICRO WIND Tool.

6. RS LATCH

Date:

Aim: To generate schematic for RS LATCH using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: A latch is a sequential device that checks all of its inputs continuously and changes its outputs accordingly at any independent of a clocking signal. RS latch uses two NAND gates, these two gates are cross coupled so that the output of a NAND gate 1 is connected to one of the input of NAND gate 2 and vice versa.

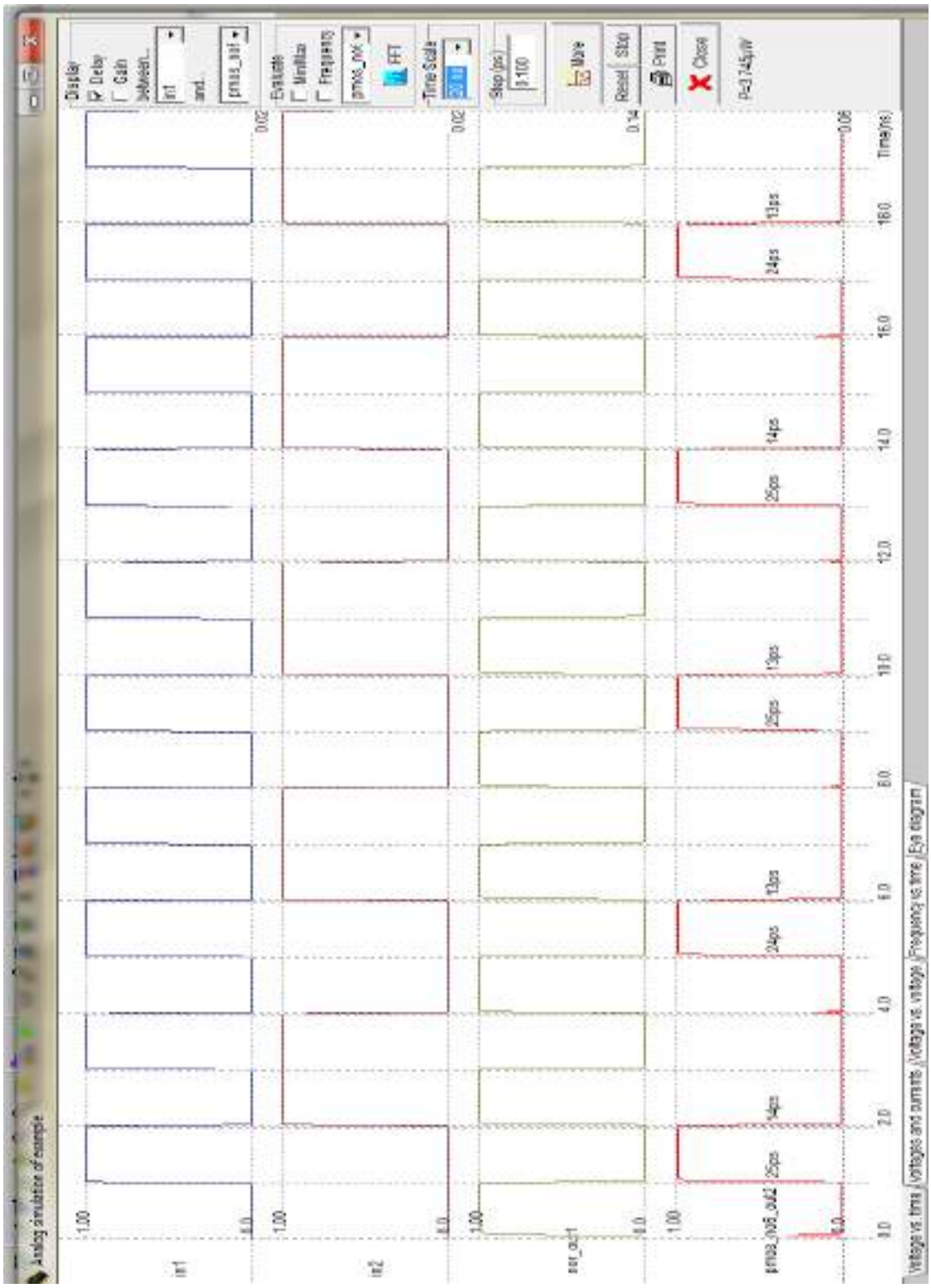
Truth Table:

S	R	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

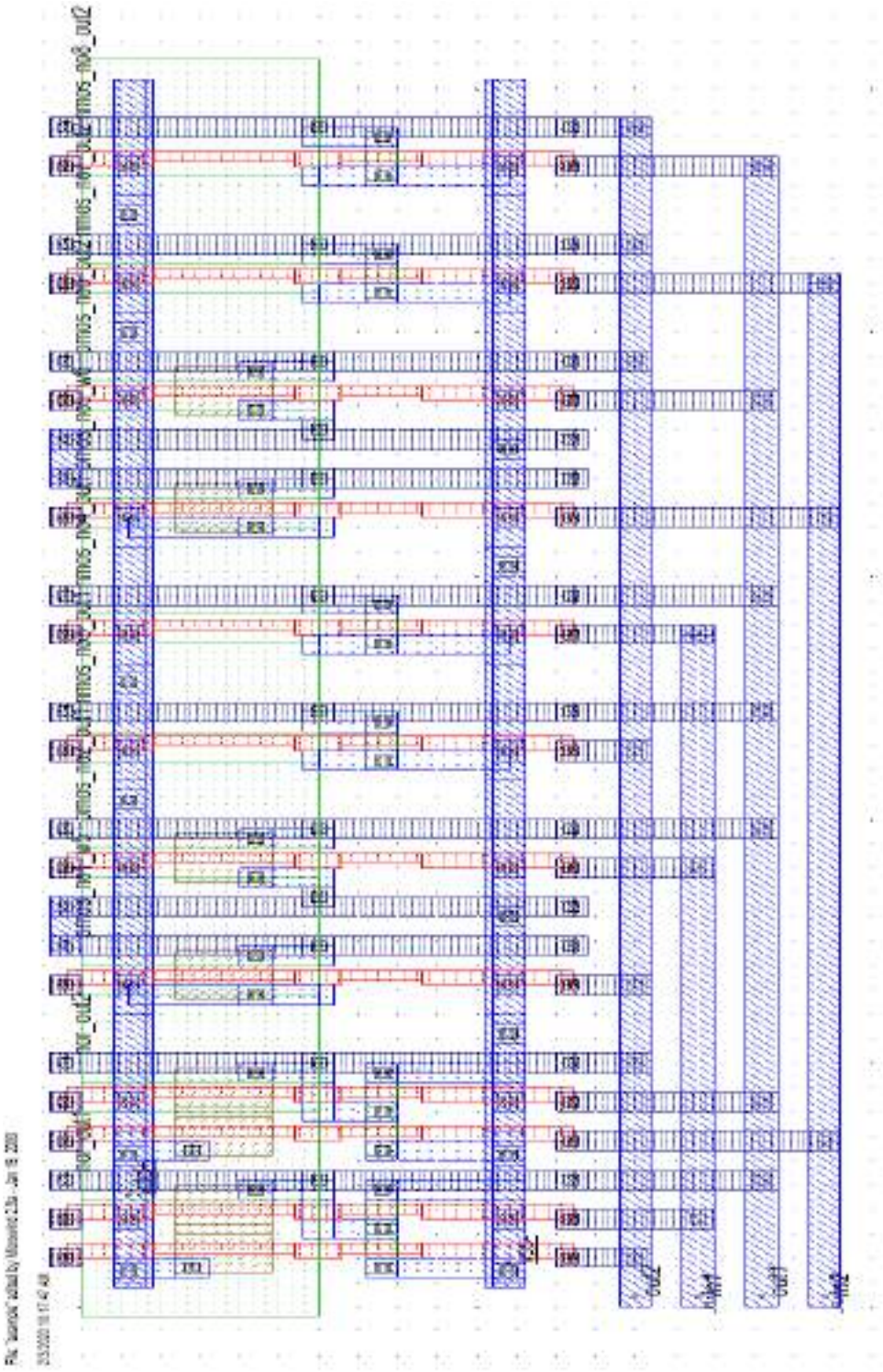
Schematic Diagram for RS Latch:

Symbol for RS Latch:

Waveforms for RS Latch:



Layout for RS LATCH:



Result: Hence simulated and verified the schematic of RS Latch using DSCH & MICRO WIND Tool.

7. D-LATCH

Date:

Aim: To generate schematic and layout for a D-Latch using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: Latch is an electronic device that can be used to store one bit of information. The D latch is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch.

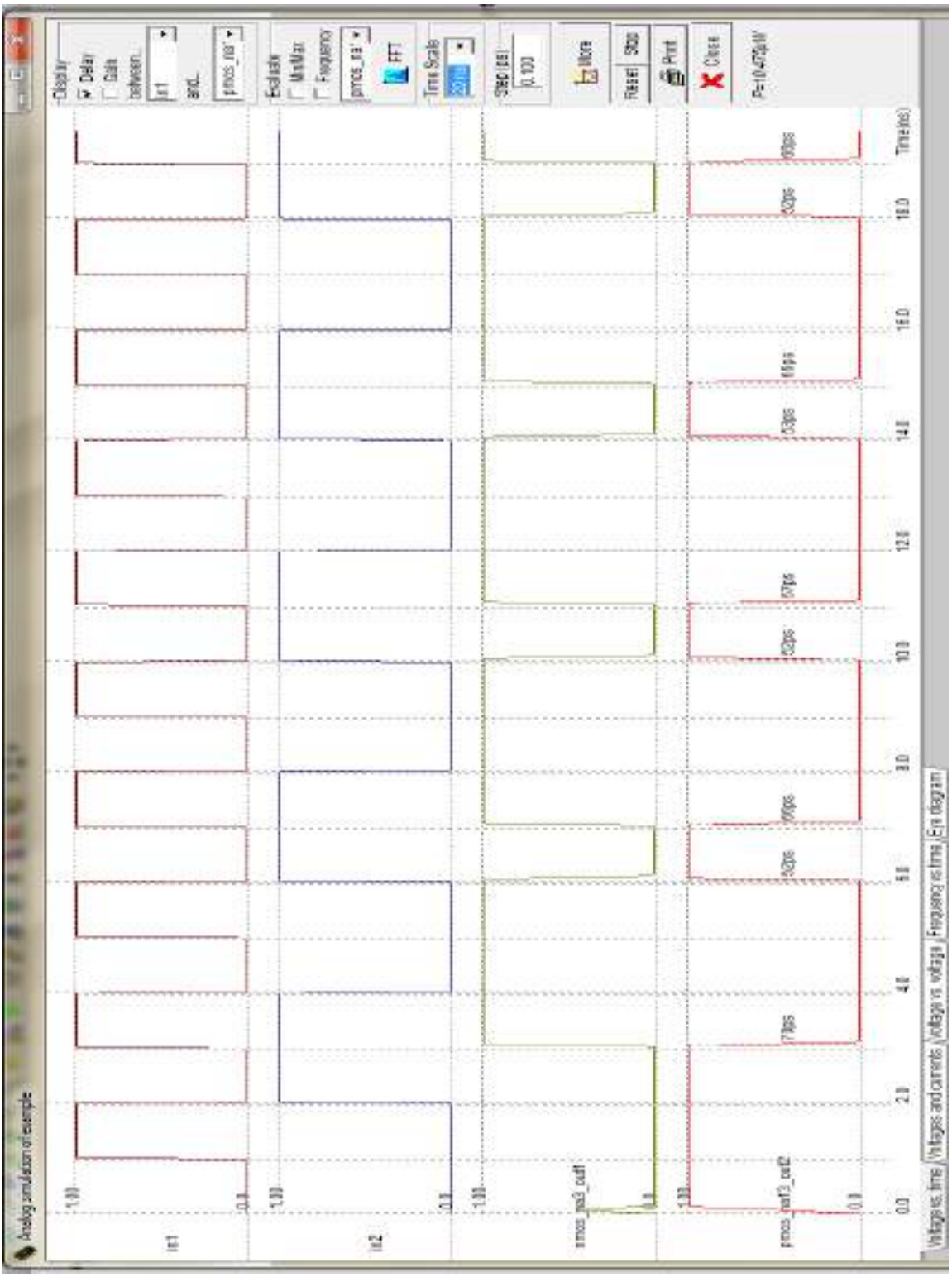
Truth Table:

CLK	D	Q	QBAR
0	0	Q	QBAR
0	1	Q	QBAR
1	0	0	1
1	1	1	0

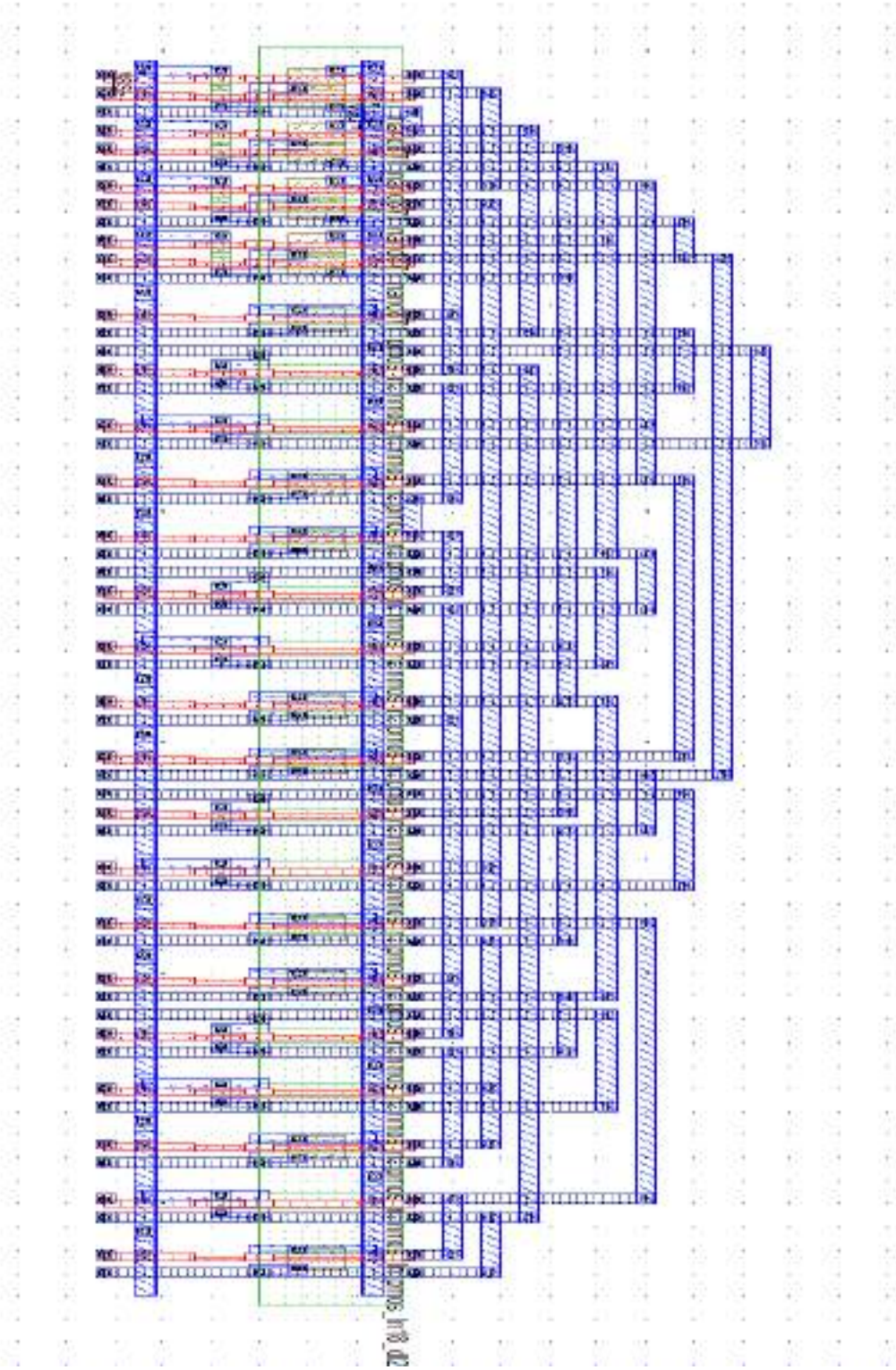
Schematic Diagram for D-Latch:

Symbol for D-Latch:

Waveforms for D-Latch:



Layout for D-LATCH:



Result: Hence simulated and verified the schematic of D-latch using mentor graphics tool.

7.2 JK FLIP FLOP

Date:

Aim: To generate schematic for a JK Flip Flop using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: JK flip Flop is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. Like the R-S flip-flop the outputs follow the inputs when the Clk is logic, but there are two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K both are high at the clock edge then the output will toggle from one state to the other.

Truth Table:

Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

Schematic Diagram for JK Flip Flop:

Symbol for JK Flip Flop:

Waveforms for JK Flip Flop:

Result: Hence simulated and verified the schematic of JK Flip Flop using DSCH & MICRO WIND Tool.

8 ASYNCHRONOUS COUNTER

Date:

Aim: To generate schematic for an Asynchronous Counter using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: Asynchronous counters are those whose output is free from the clock signal. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be delay in producing output. The required number of logic gates to design asynchronous counters is very less. So they are simple in design. Another name for Asynchronous counters is "Ripple counters". The rising edge of the Q output of each flip flop triggers the clock input of its next flip flop.

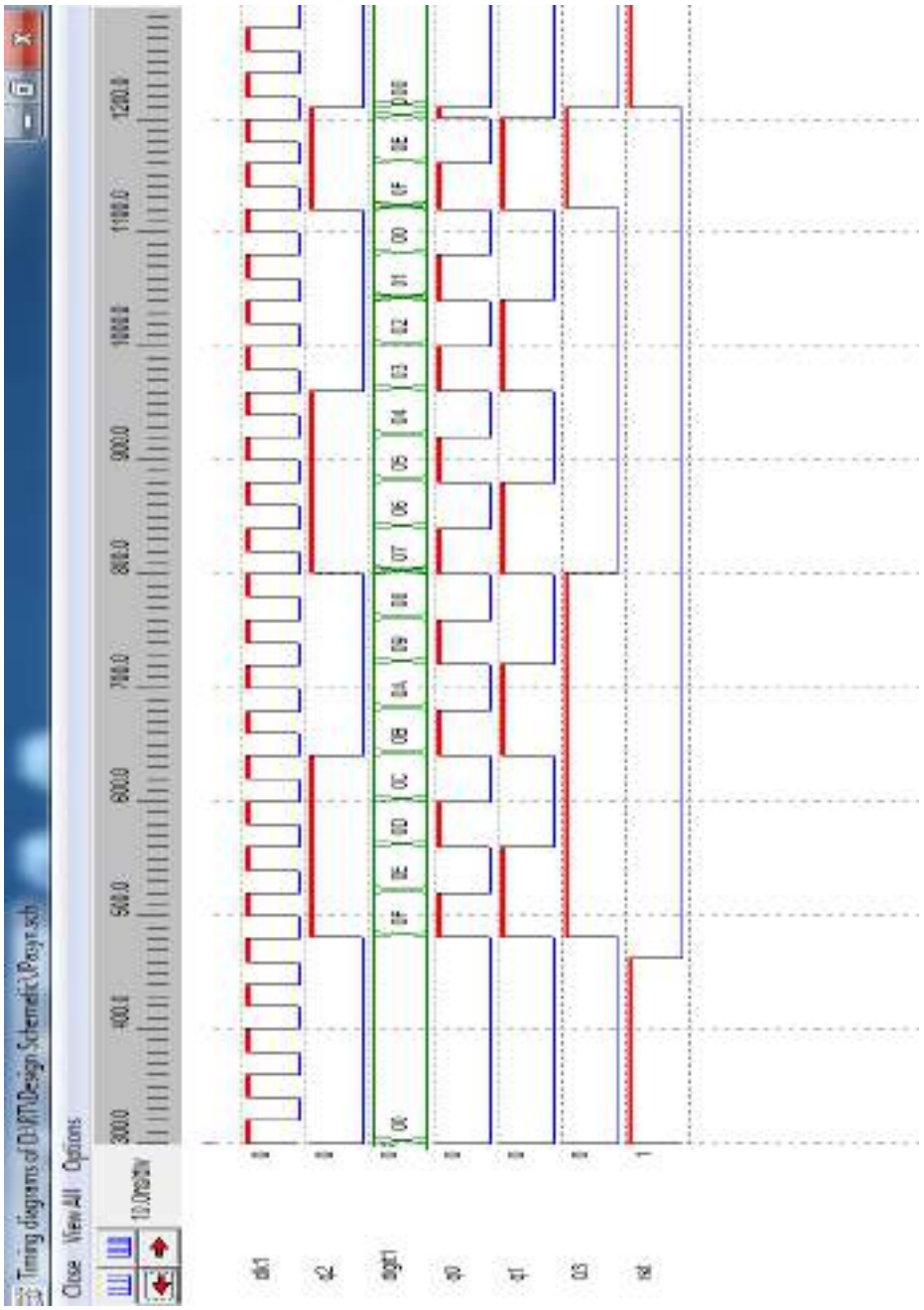
Truth Table:

CK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

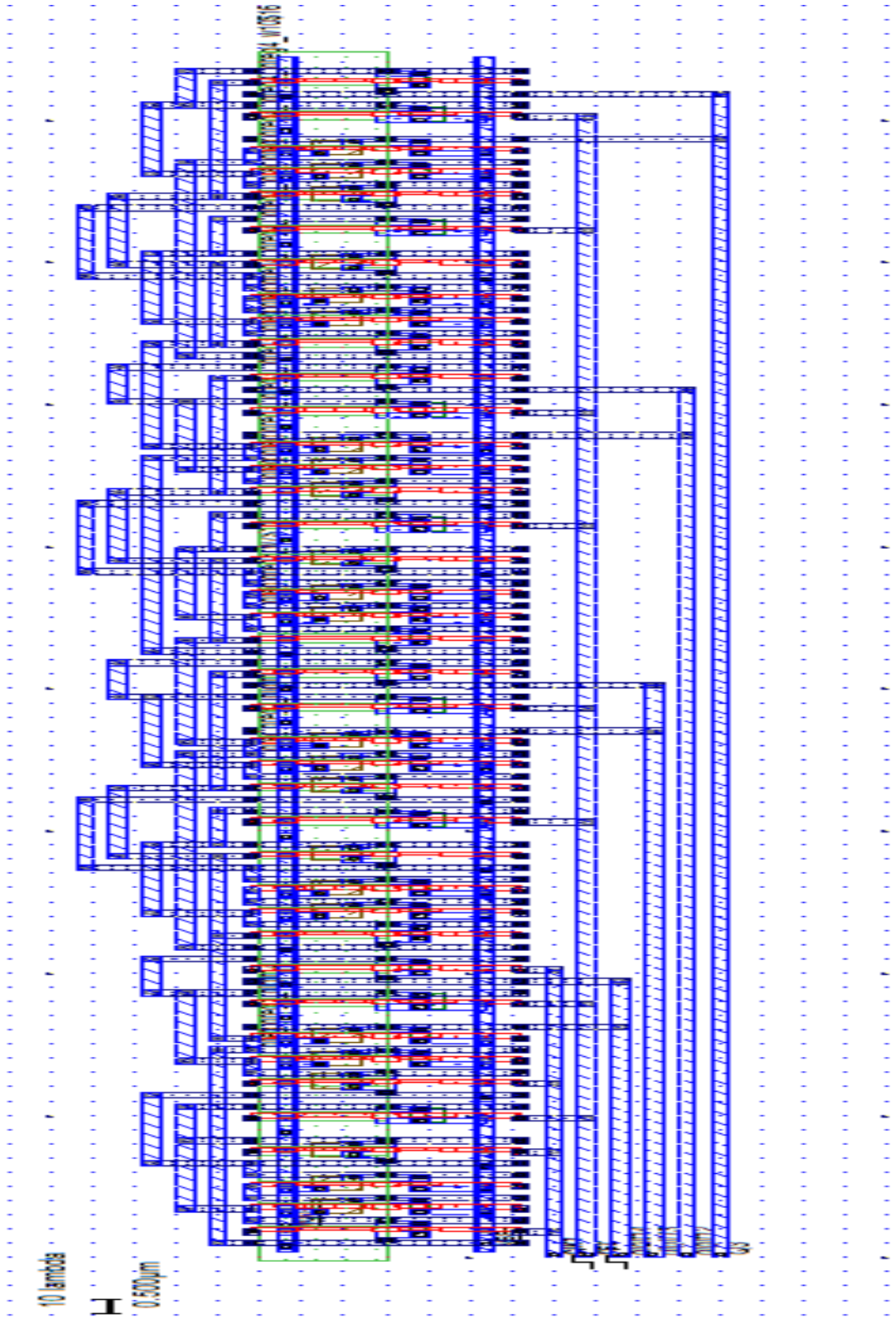
Schematic Diagram for Asynchronous Counter:

Symbol for Asynchronous Counter:

Waveforms for Asynchronous Counter:



Layout for Asynchronous Counter:



Result: Hence simulated and verified the schematic of Asynchronous Counter using DSCH & MICRO WIND Tool.

9. STATIC RAM

Date:

Aim: To generate schematic for a Static RAM using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory: A Random Access Memory (RAM) or Read Write Memory (RWM) is equal to a group of address registers. The static RAM uses bipolar or MOS flip-flops. Data is retained indefinitely as long as power is applied to the flip flops.

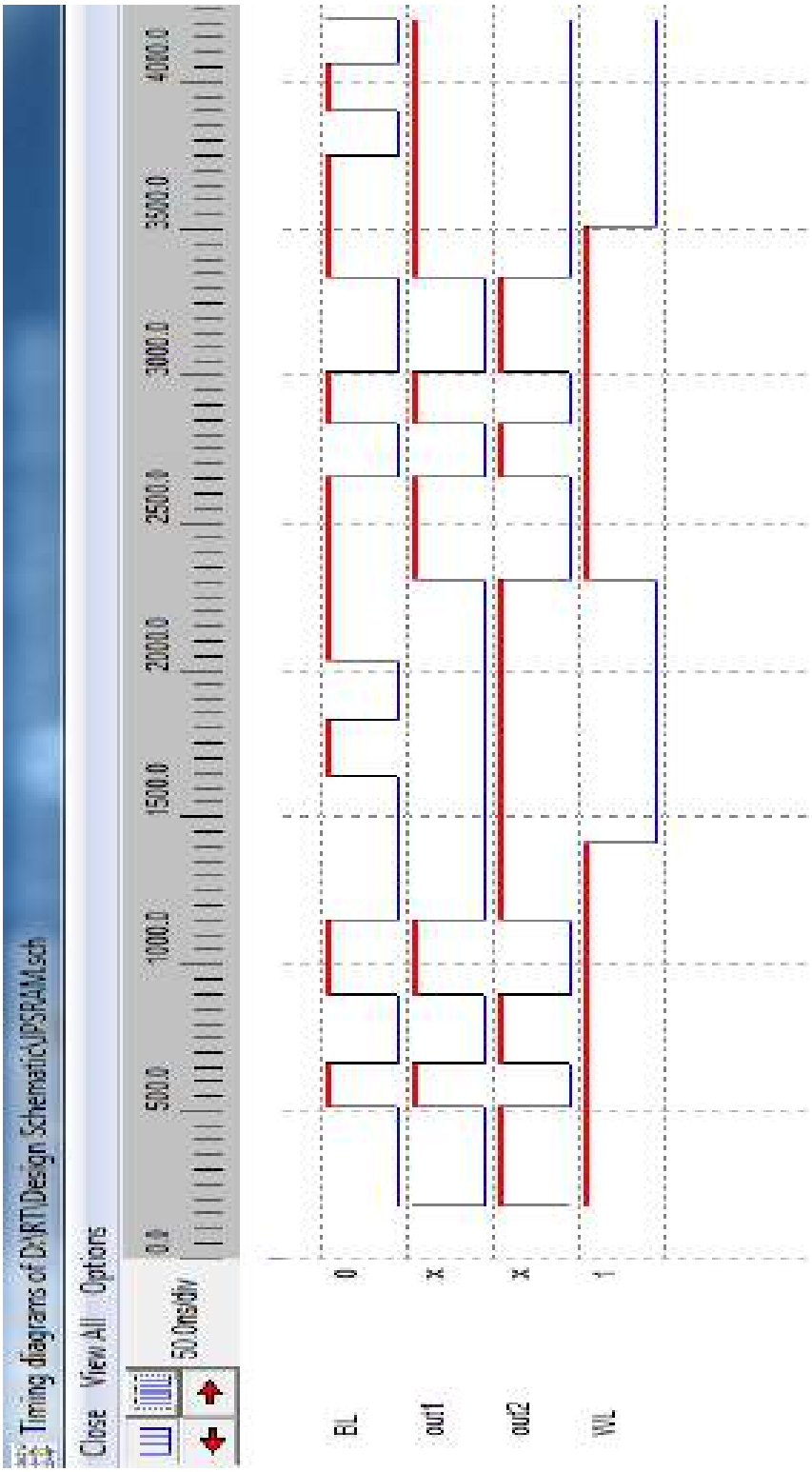
Truth Table:

WL	BL	$\overline{WL}$	Q	$\bar{Q}$
0	0	1	0	1
1	0	1	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	1	0

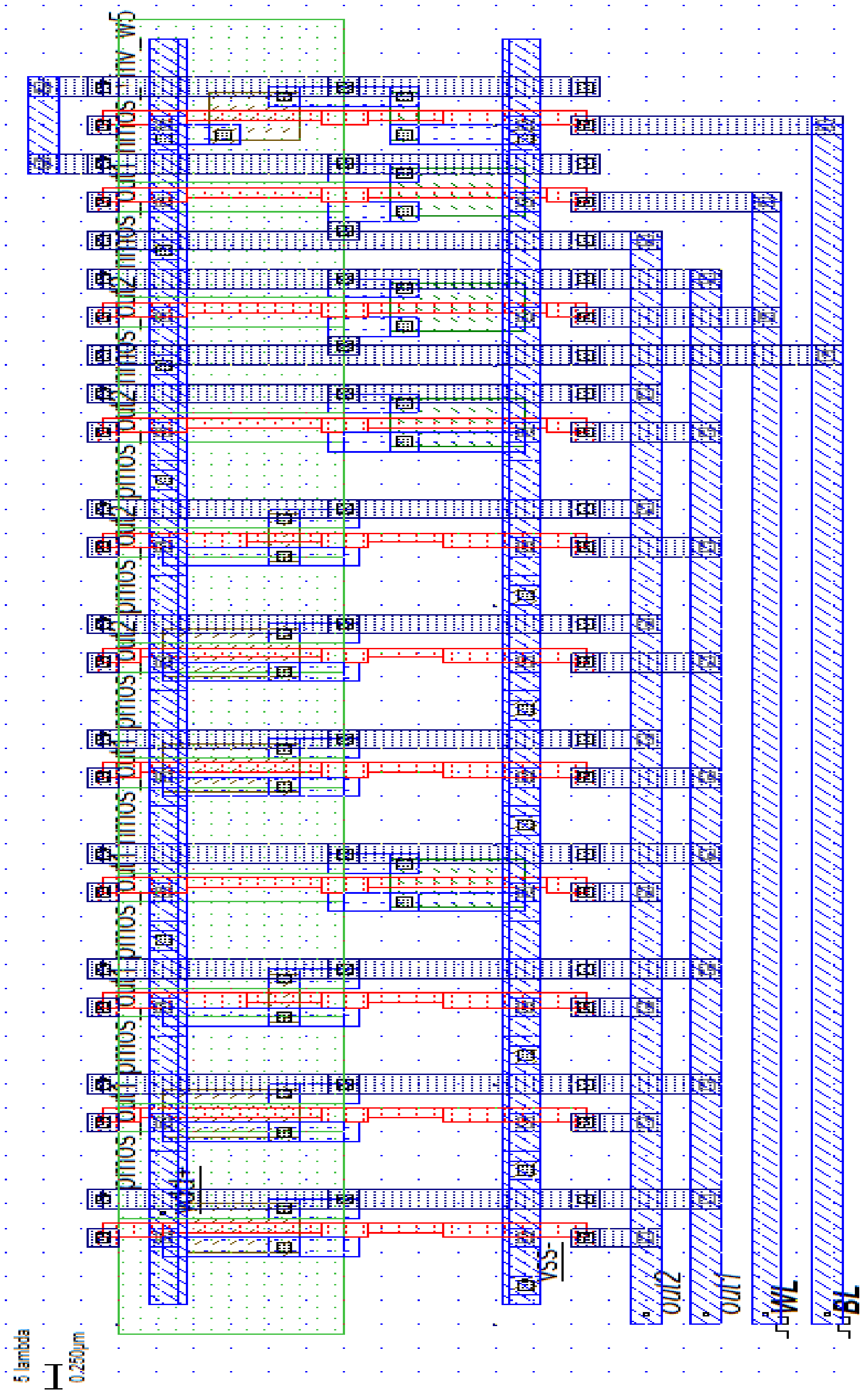
Schematic Diagram for Static RAM:

Symbol for Static RAM:

Waveforms for Static RAM:



Layout for Static RAM:



Result: Hence simulated and verified the schematic of Static RAM using DSCH & MICRO WIND Tool.

10. MULTIPLEXER

Date:

Aim: To generate schematic for 8 x1 Multiplexer using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

2. Software: DSCH & MICRO WIND Tool

Theory:

Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input.

8x1 Multiplexer

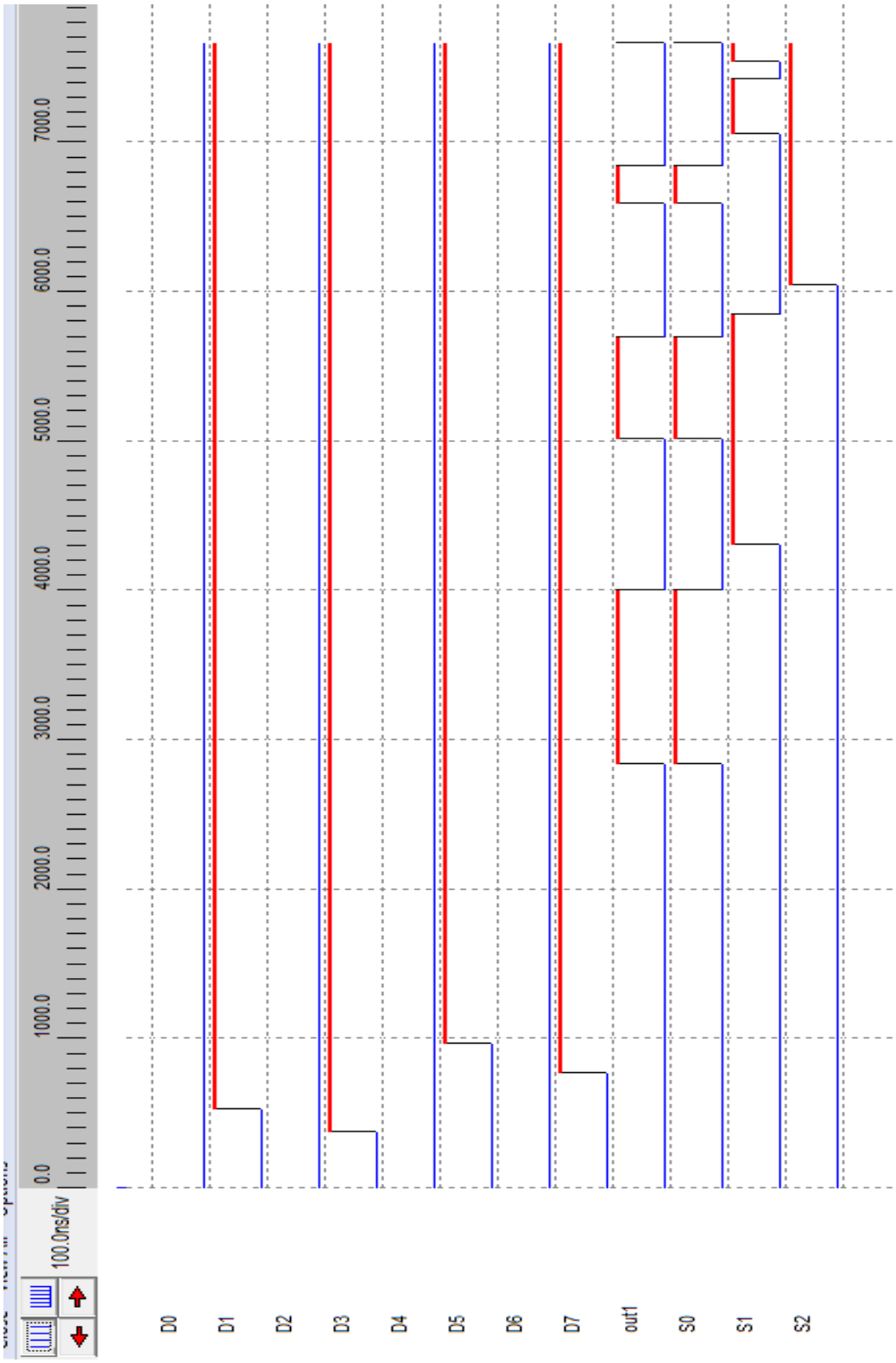
We implement 8x1 Multiplexer using 4x1 Multiplexers and 2x1 Multiplexer. We know that 4x1 Multiplexer has 4 data inputs, 2 selection lines and one output. Whereas, 8x1 Multiplexer has 8 data inputs, 3 selection lines and one output. So, we require two 4x1 Multiplexers in first stage in order to get the 8 data inputs. Since, each 4x1 Multiplexer produces one output, we require a 2x1 Multiplexer in second stage by considering the outputs of first stage as inputs and to produce the final output. Let the 8x1 Multiplexer has eight data inputs I_7 to I_0, three selection lines s_2, s_1 & s0 and one output Y.

S(2)	S(1)	S(0)	Y
0	0	0	I(0)
0	0	1	I(1)
0	1	0	I(2)
0	1	1	I(3)
1	0	0	I(4)
1	0	1	I(5)
1	1	0	I(6)
1	1	1	I(7)

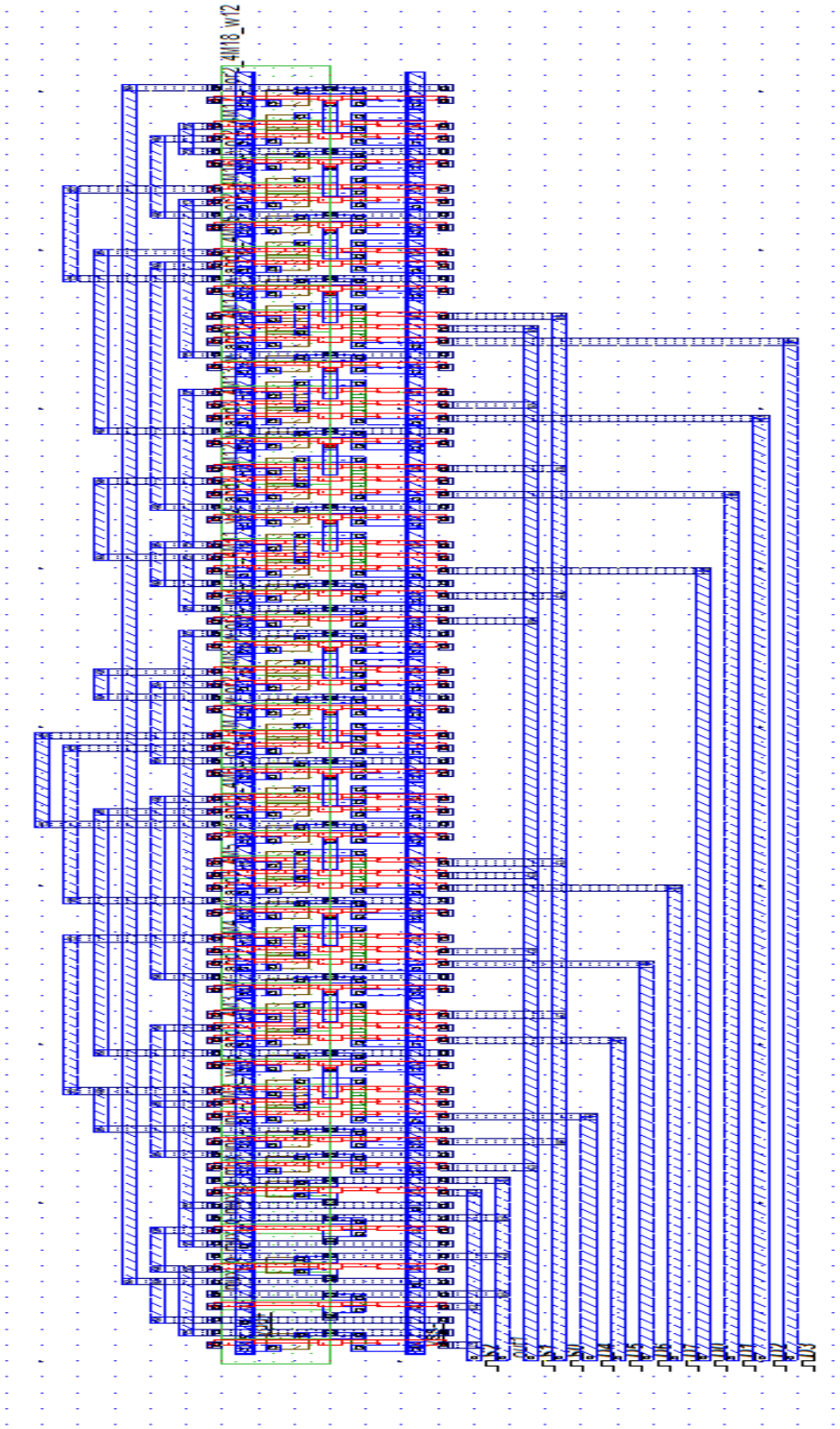
Schematic Diagram for 8x1 MUX:

Symbol for 8x1 MUX :

Waveform for 8x1 MUX



Layout for 8x1 MUX :



Result: Hence simulated and verified the schematic of 8 x1 Multiplexer using DSCH & MICRO WIND Tool.

11. DIFFERENTIAL AMPLIFIER

Date:

Aim: To generate schematic Differential Amplifier using DSCH & MICRO WIND Tool.

Tools Required:

1. Operating System: Windows XP

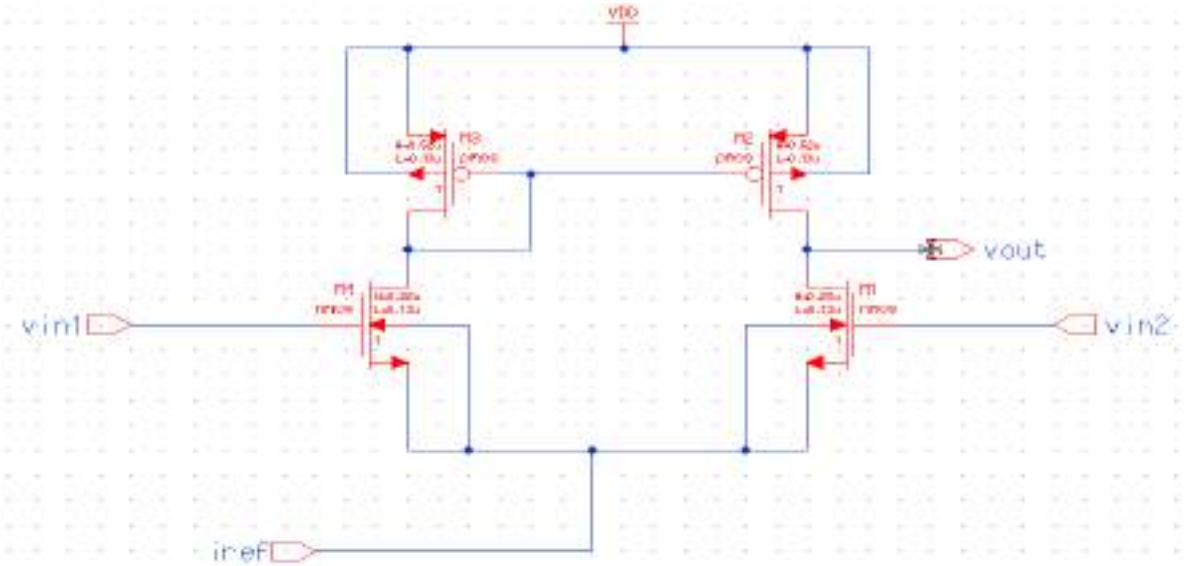
2. Software: DSCH & MICRO WIND Tool

Theory: A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. It is an analog circuit with two inputs Vin1 and Vin2 and one output Vout in which the output is ideally proportional to the difference between the two voltages.

$$Vout = A (Vin2 - Vin1)$$

Where A is the Gain of the Amplifier.

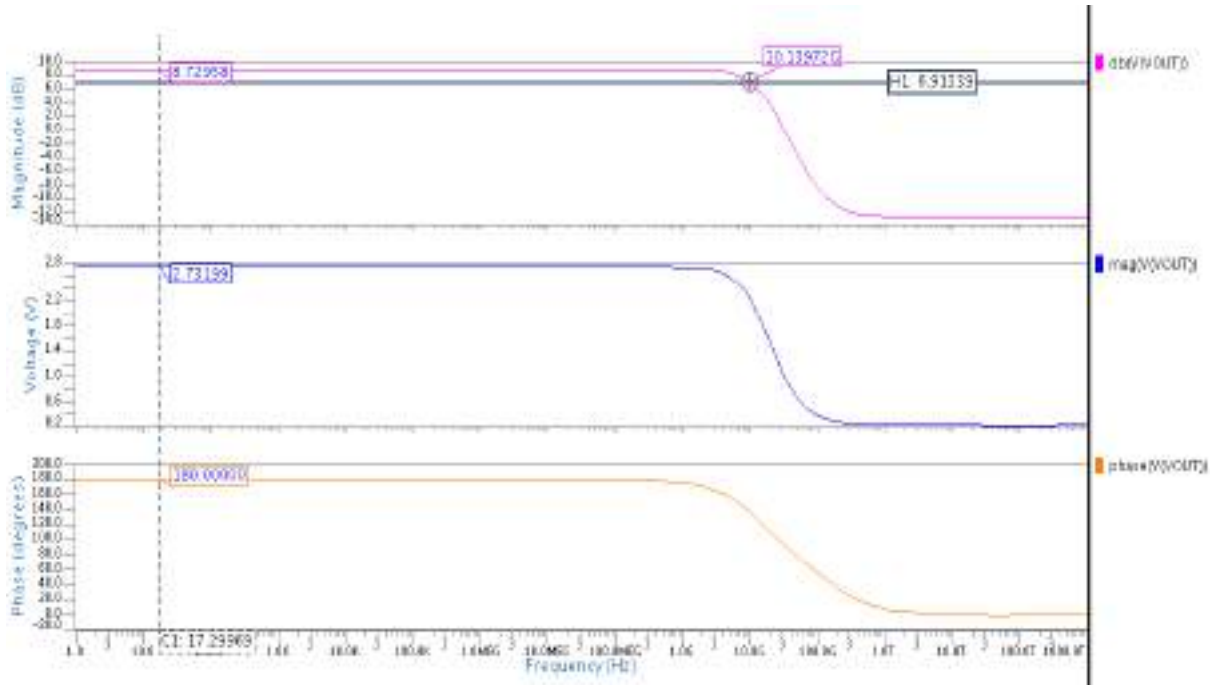
Schematic Diagram for Differential Amplifier:



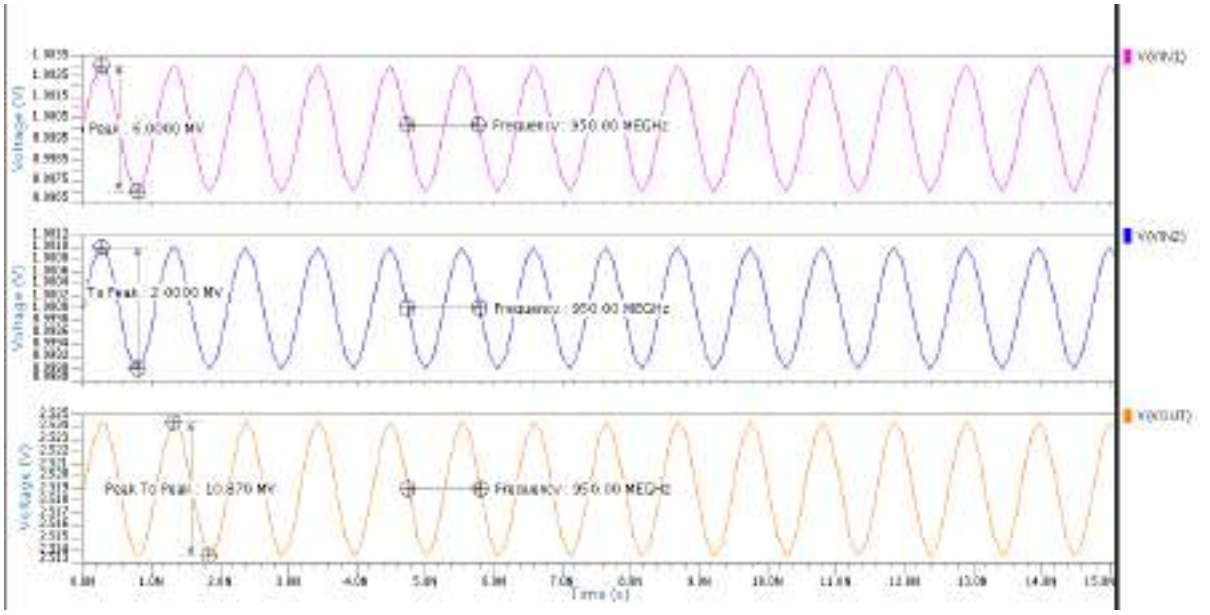
Symbol for Differential Amplifier:

Simulation Diagram for Differential Amplifier:

AC Analysis



Transit Analysis



Result: Hence simulated and verified the schematic of Differential Amplifier using DSCH & MICRO WIND Tool.