# ELECTRONIC DEVICES CIRCUITS (EDC)

# LABORATORY MANUAL

## FOR II / IV B.E (ECE) : I – SEMESTER (R19)


**DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING**

## SIR C.R.REDDY COLLEGE OF ENGINEERING

## ELURU – 534 007

# ELECTRONIC DEVICES CIRCUITS (EDC) - LAB

## FOR II/IV B.Tech (ECE), I - SEMESTER

## LIST OF EXPERIMENTS

**Note:** The students are required to perform the experiment to obtain the V-I characteristics and to determine the relevant parameters from the obtained graphs.

**Electronic Workshop Practice:**
1. Identification, Specifications, Testing of R, L, C Components (Colour Codes), Potentiometers, Coils, Gang Condensers, Relays, Bread Boards.
2. Identification, Specifications and Testing of active devices, Diodes, BJTs, JFETs, LEDs, LCDs, SCR, UJT.
3. Soldering Practice- Simple circuits using active and passive components.
4. Study and operation of Ammeters, Voltmeters, Transformers, Analog and Digital Multimeter, Function Generator, Regulated Power Supply and CRO..

**List of Experiments: (Minimum of Ten Experiments has to be performed)**

1. **PN JUNCTION DIODE CHARACTERISTICS**
   Part-A: Germanium Diode (FB & RB)
   Part-B: Silicon Diode (FB)
2. **ZENER DIODE CHARACTERISTICS**
   Part-A: V-I Characteristics
   Part-B: Zener Diode as a Voltage Regulator
3. **RECTIFIERS (Without and With Capacitor Filter)**
   Part-A: Half-Wave Rectifier
   Part-B: Full-Wave Rectifier (Centre tapped)
   Part-C: Full-Wave Bridge Rectifier
4. **BJT CHARACTERISTICS (CB / CE)**
   Part-A: Input Characteristics
   Part-B: Output Characteristics
5. **FET CHARACTERISTICS (CS Configuration)**
   Part-A: Drain Characteristics
   Part-B: Transfer Characteristics
6. **TRANSISTOR BIASING -** Design Self Bias Circuit
7. **CRO OPERATION AND ITS MEASUREMENTS**
8. **BJT CE AMPLIFIER**
9. **EMITTER FOLLOWER – CC AMPLIFIER**
10. **FET-CS AMPLIFIER**
11. **CHARACTERISTICS OF UJT**
12. **SCR CHARACTERISTICS**
13. **TRANSISTOR AS A SWITCH**

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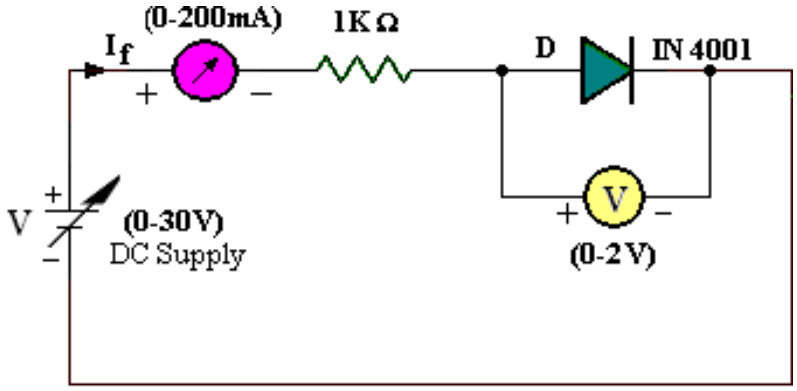
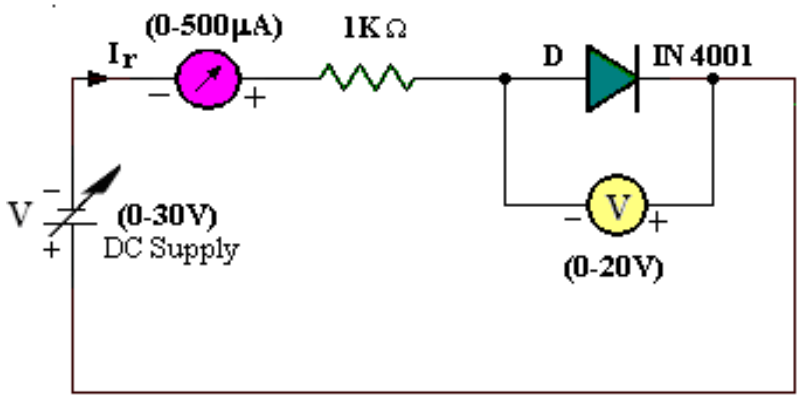
**CIRCUIT DIAGRAMS:**

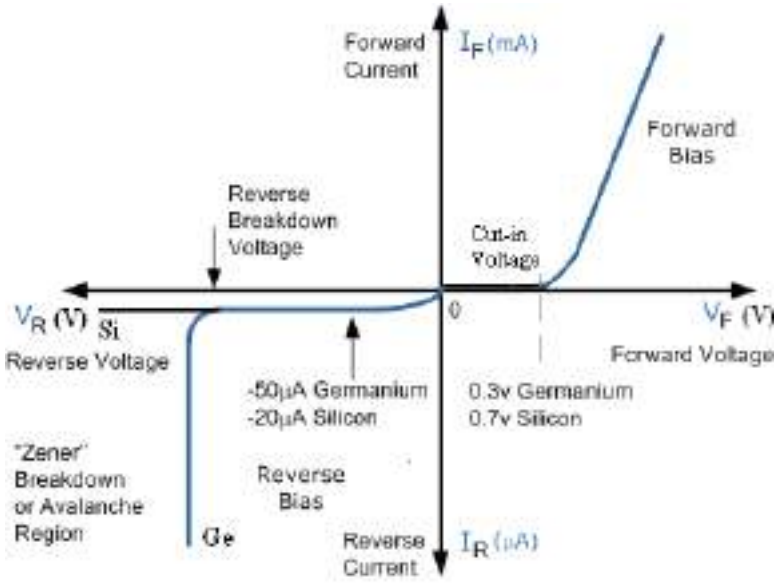



Forward Bias Characteristics




Reverse Bias Characteristics

**MODEL GRAPH:**




V-I Characteristics of PN Junction Diode

# 1. PN JUNCTION DIODE CHARACTERISTICS

**Exp. No:…….** **Date:……**

**AIM:** 1. To Plot the Volt Ampere Characteristics of PN Junction Diode under Forward and Reverse Bias Conditions.

**2.** To find the Cut-in voltage, Static Resistance, Dynamic Resistance for Forward Bias & Reverse Bias

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | DC Regulated Power Supply | 0 – 30 volts | 1 |
| 2 | Diode | 1N 4001 | 1 |
| 3 | Diode | OA 82 | 1 |
| 4 | Resistor | 1KΩ | 1 |
| 5 | D.C Ammeters | 0–100mA, 0–500μA | Each 1 |
| 6 | D.C Volt meters | 0–2V, 0–20V | Each 1 |
| 7 | Bread Board and connecting wires | - | 1 Set |

**THEORY:**

The semi conductor diode is created by simply joining an n-type and a p-type material together nothing more just the joining of one material with a majority carrier of electrons to one with a majority carrier of holes.

The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to anode (P-side) and –ve terminal of the input supply is connected to cathode (N- side), then diode is said to be forward biased. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current( injected minority current – due to holes crossing the junction and entering N-side of the diode, due to electrons crossing the junction and entering P-side of the diode).

Assuming current flowing through the diode to be very large, the diode can be approximated as short-circuited switch. If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on p-side and electrons on n-side tend to move away from the junction thereby increasing the depleted region. However the

process cannot continue indefinitely, thus a small current called **reverse saturation current**continues to flow in the diode. This small current is due to thermally generated carriers. Assuming current flowing through the diode to be negligible, the diode can be approximated as an open circuited switch.

The volt-ampere characteristics of a diode explained by following equation:

$$I = I_0 \left(e^{\eta \frac{V}{V_T}} - 1\right)$$

I=current flowing in the diode $I_0$=reverse saturation current V=voltage applied to the diode

$V_T$=volt-equivalent of temperature = 26mv
$\eta = 1$ (for Ge)
$\eta = 2$ (for Si)

It is observed that Ge diode has smaller cut-in-voltage when compared to Si diode. The reverse saturation current in Ge diode is larger in magnitude when compared to silicon diode.

**PROCEDURE:**

**FORWARD BIAS CHARACTERISTICS**:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power Supply and slowly increase the source voltage. Increase the Diode Current in steps of 2mA and note down the corresponding voltage across the PN junction Diode under forward Bias condition as per table given below.
3. Take the readings until a Diode Current of 30mA.
4. Repeat the same by using Ge Diode instead of Si Diode.
5. Plot the graph $V_F$ versus $I_F$ on the graph Sheet in the 1st quadrant as in Fig.
6. From the graph find out the Static & Dynamic forward Bias resistance of the diode

$$R = \frac{V_F}{I_F}, \qquad r_{ac} = \frac{\Delta V_F}{\Delta I_F}.$$

7. Observe and note down the cut in Voltage of the diode.

**REVERSE BIAS CHARACTERISTICS:**

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power Supply and slowly increase the source voltage. Increase the Diode voltage in steps of 2.0 volts and note down the corresponding

Current against the Voltage under Reverse Bias condition as per table given below.

3. Take readings until a Diode Voltage reaches 30.0V.
4. Repeat the same by using Ge Diode instead of Si Diode.
5. Plot the graph $V_R$ versus $I_R$ on the graph Sheet in the 3rd quadrant as in Fig.
6. From the graph find out the Dynamic Reverse Bias resistance of the diode.

$$R = \frac{V_R}{I_R}, \qquad r_{ac} = \frac{\Delta V_R}{\Delta I_R}.$$

7. Observe and note down the break down Voltage of the diode.

**RESULT :**

The V-I Characteristics of the PN Junction Diode are plotted for the both Forward and Reverse Bias conditions and Calculated the Cut in Voltage, Dynamic Forward and Reverse Bias resistance.

| **Specifications** | | **Si** | **Ge** |
|---|---|---|---|
| Cut in Voltage | | | |
| Static Resistance | F. Bias | | |
| | R. Bias | | |
| Dynamic Resistance | F. Bias | | |
| | R. Bias | | |

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

**VIVA QUESTIONS:**

1. Draw the circuit symbol of the Diode?

2. What are the materials used for Anode and Cathode?

3. Draw ideal Diode Volt Ampere Characteristics?

4. What is Cut in Voltage?

**TABULAR FORMS:**

**FORWARD BIAS**:

| S.No | Voltmeter Reading $V_F$(Volts) | | Ammeter Reading $I_F$ (mA) |
|---|---|---|---|
| | Ge | Si | |
| 1 | | | 0.0 |
| 2 | | | 0.2 |
| 3 | | | 0.6 |
| 4 | | | 2 |
| 5 | | | 4 |
| 6 | | | 6 |
| 7 | | | 8 |
| 8 | | | 10 |
| 9 | | | 14 |
| 10 | | | 18 |
| 11 | | | 20 |

**REVERSE BIAS**:

| Voltmeter Reading $V_R$ (Volts) | Ammeter Reading $I_R$ (mA/μA) | |
|---|---|---|
| | Ge | Si |
| 0 | | |
| 2 | | |
| 4 | | |
| 6 | | |
| 8 | | |
| 10 | | |
| 12 | | |
| 14 | | |
| 16 | | |
| 18 | | |
| 20 | | |

5. Explain the working of a Diode as a switch

6. What is space charge?

7. What is Diffusion Capacitance?

8. What are Minority and Majority carriers in P type and in N type materials?

9. What are the specifications of a Diode?

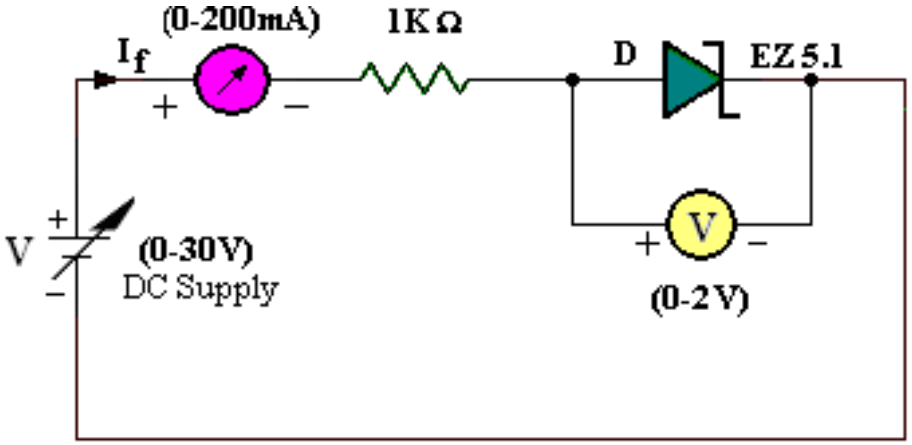
10. What is PIV?

11. Why leakage current is more for Ge Diode?

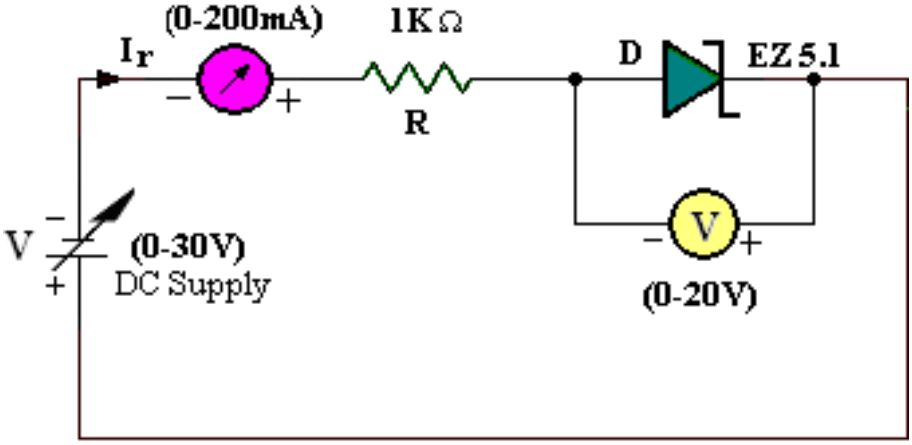
12. What is work function?

13. What is the current equation of the Diode?

**CIRCUIT DIAGRAMS:**

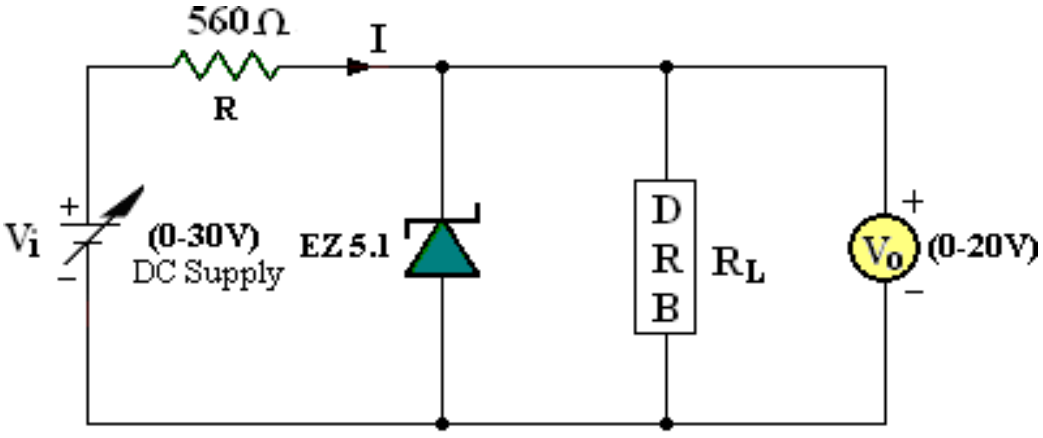



Forward Bias Characteristics




Reverse Bias Characteristics

**VOLTAGE REGULATION:**




Zener Diode Voltage Regulation

# 2. ZENER DIODE CHARACTERISTICS

**Exp.No:…….** **Date:…….**

**AIM:** i) To Obtain the Forward Bias and Reverse Bias characteristics of a Zener diode.
ii) Find out the Zener Break down Voltage from the Characteristics.
iii) To Obtain the Load Regulation Characteristics.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | DC Regulated Power Supply | 0 – 30 volts | 1 |
| 2 | Diode | ECZ 5.1 | 1 |
| 3 | Resistor | 1KΩ, 560Ω | Each 1 |
| 4 | D.C Ammeters | 0–200mA | 1 |
| 5 | D.C Volt meters | 0–2V, 0–20V | Each 1 |
| 6 | Decade Resistance Box | - | 1 |
| 7 | Bread Board and connecting wires | - | 1 Set |

**THEORY:**

An ideal P-N Junction diode does not conduct in reverse biased condition. A zener diode conducts excellently even in reverse biased condition. These diodes operate at a precise value of voltage called break down voltage. A zener diode when forward biased behaves like an ordinary P-N junction diode.

A zener diode when reverse biased can either undergo avalanche break down or zener break down. Avalanche break down:-If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction may rupture covalent bonding between electrons. Such rupture leads to the generation of a large number of charge carriers resulting in avalanche multiplication.

Zener break down:-If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces. Application of even a small voltage at the junction ruptures covalent bonding and generates large number of charge carriers. Such sudden increase in the number of charge carriers results in zener mechanism.

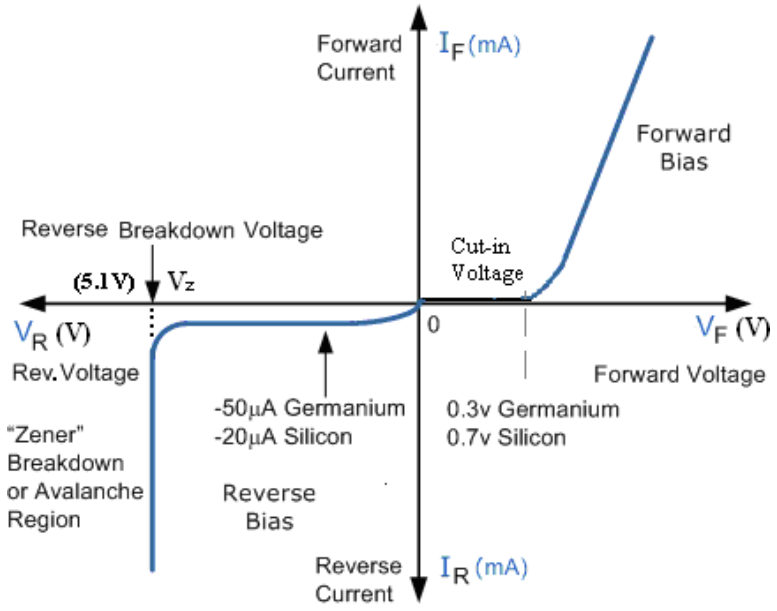
**PROCEDURE:**

**FORWARD BIAS CHARACTERISTICS**:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power Supply and slowly increase the source voltage. Increase the Diode Current in steps of 2mA and note down the corresponding voltage across the Zener Diode under forward Bias condition as per table given below.
3. Take the readings until a Diode Current of 20mA.

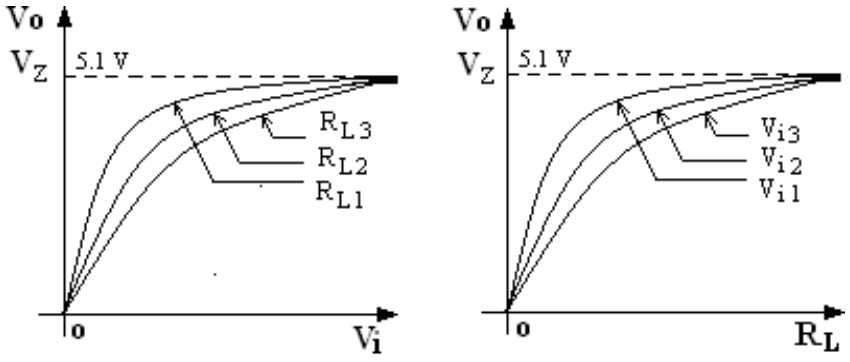
**MODEL GRAPHS:**

**ZENER DIODE CHARACTERISTICS**:




V-I Characteristics of Zener Diode

**LOAD REGULATION CHARACTERISTICS**:




Voltage Rgulation Charastics Vi vs Vo and $R_L$ vs Vo

4. Plot the graph $V_F$ versus $I_F$ on the graph Sheet in the 1st quadrant as in Fig.
5. From the graph find out the Static & Dynamic forward Bias resistance of the diode

$$R = \frac{V_F}{I_F}, \qquad r_{ac} = \frac{\Delta V_F}{\Delta I_F}.$$

**REVERSE BIAS CHARACTERISTICS:**

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power Supply and slowly increase the source voltage. Increase the Diode Current in steps of 2mA and note down the corresponding voltage across the Zener Diode under Reverse Bias condition as per table given below.
3. Take the readings until a Diode Current of 20mA.
4. Plot the graph $V_R$ versus $I_R$ on the graph Sheet in the 3rd quadrant as in Fig.
5. From the graph find out the Dynamic Reverse Bias resistance of the diode.

$$R = \frac{V_R}{I_R}, \qquad r_{ac} = \frac{\Delta V_R}{\Delta I_R}.$$

7. Observe and note down the break down Voltage of the diode.

**LOAD REGULATION CHARACTERISTICS**:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. By changing the load Resistance, kept constant I/P Voltage at 5V, 10 V, 15 V as per table given below. Take the readings of O/P Voltmeter (Vo=Vz).
3. Now by changing the I/P Voltage, kept constant load Resistance at 1K, 2K, 3K as per table given below. Take the readings of O/P Voltmeter (Vo=Vz).

**ZENER BREAKDOWN VOLTAGE:**

Draw a tangent on the reverse Bias Characteristic of the Zener Diode starting from the Knee and touching most of the points of the curve. The point where the tangent intersects the X-axis is the Zener Breakdown Voltage.

**RESULT:**

The Characteristics of the Forward and Reverse biased Zener Diode and the Zener Break Down Voltage from the Characteristics are Observed.

Zener Breakdown Voltage = Volts.

Forward Bias Resistance = Ohms

Reverse Bias Resistance = Ohms

**TABULAR FORMS:**

**FORWARD BIAS**:

| S.No | Voltmeter Reading $V_F$(Volts) | Ammeter Reading $I_F$ (mA) |
|---|---|---|
| 1 | | 0.0 |
| 2 | | 0.2 |
| 3 | | 0.4 |
| 4 | | 0.6 |
| 5 | | 0.8 |
| 6 | | 2 |
| 7 | | 4 |
| 8 | | 6 |
| 9 | | 8 |
| 10 | | 10 |
| 11 | | 12 |
| 12 | | 16 |
| 13 | | 18 |
| 14 | | 20 |

**REVERSE BIAS**:

| Voltmeter Reading $V_R$ (Volts) | Ammeter Reading $I_R$ (mA) |
|---|---|
| | 0.0 |
| | 0.2 |
| | 0.4 |
| | 0.6 |
| | 0.8 |
| | 2 |
| | 4 |
| | 6 |
| | 8 |
| | 10 |
| | 12 |
| | 16 |
| | 18 |
| | 20 |

**LINE AND LOAD REGULATIONS:**

| S.No | $R_L$ (Ω) | $V_{i1}$= 5V | $V_{i2}$= 10V | $V_{i3}$=15V |
|---|---|---|---|---|
| | | $V_O$ (V) | $V_O$ (V) | $V_O$ (V) |
| 1 | 100 | | | |
| 2 | 300 | | | |
| 3 | 500 | | | |
| 4 | 700 | | | |
| 5 | 900 | | | |
| 6 | 1K | | | |
| 7 | 3K | | | |
| 8 | 5K | | | |
| 9 | 7K | | | |
| 10 | 10K | | | |

| Vi (V) | $R_{L1}$=1KΩ | $R_{L2}$=2KΩ | $R_{L3}$=3KΩ |
|---|---|---|---|
| | $V_O$ (V) | $V_O$ (V) | $V_O$ (V) |
| 0 | | | |
| 1 | | | |
| 3 | | | |
| 5 | | | |
| 7 | | | |
| 9 | | | |
| 11 | | | |
| 13 | | | |
| 15 | | | |
| 20 | | | |

**VIVA QUESTIONS:**

1. Draw the circuit symbol of the Zener Diode

2. What is meant by Zener break down?

3. What are the different types of break downs?

4. What is the difference between Avalanche Zener break down?

5. In a lightly doped and heavily doped diode which type of break down occurs?

6. Why Zener break down and Avalanche BD voltage increase with temperature?

7. What are the applications of Zener diode?

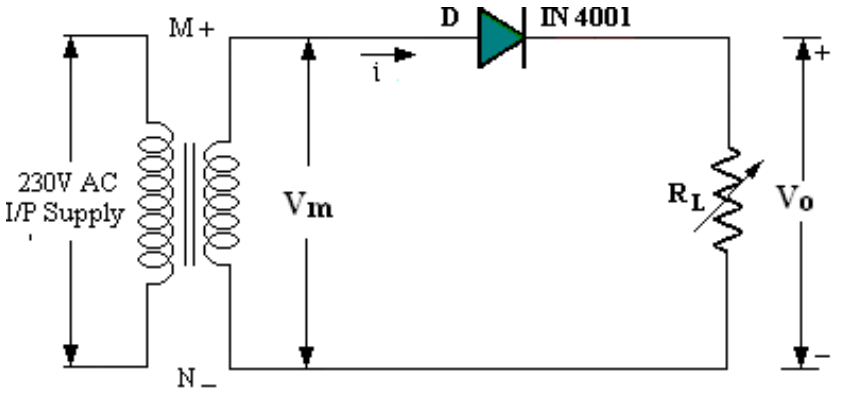
8. Explain operation of Zener diode as Voltage Regulator?

9. What is the difference between normal PN Jn diode and Zener diode?

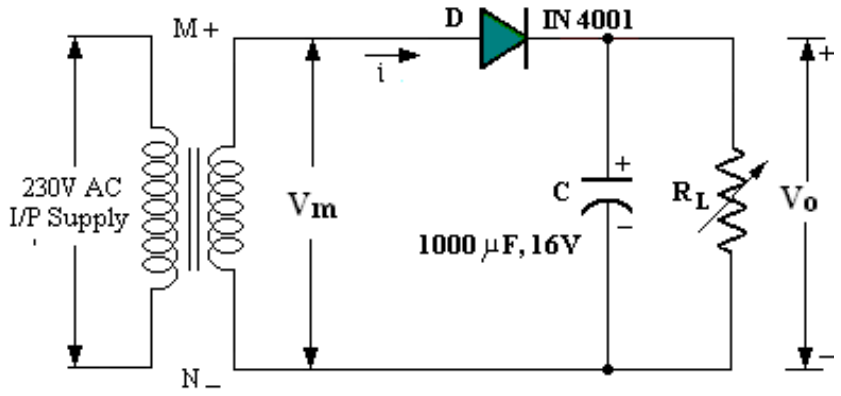
10 What is a Regulation?

**CIRCUIT DIAGRAM:**

**WITHOUT CAPACITOR FILTER AND WITH CAPACITOR FILTER:**

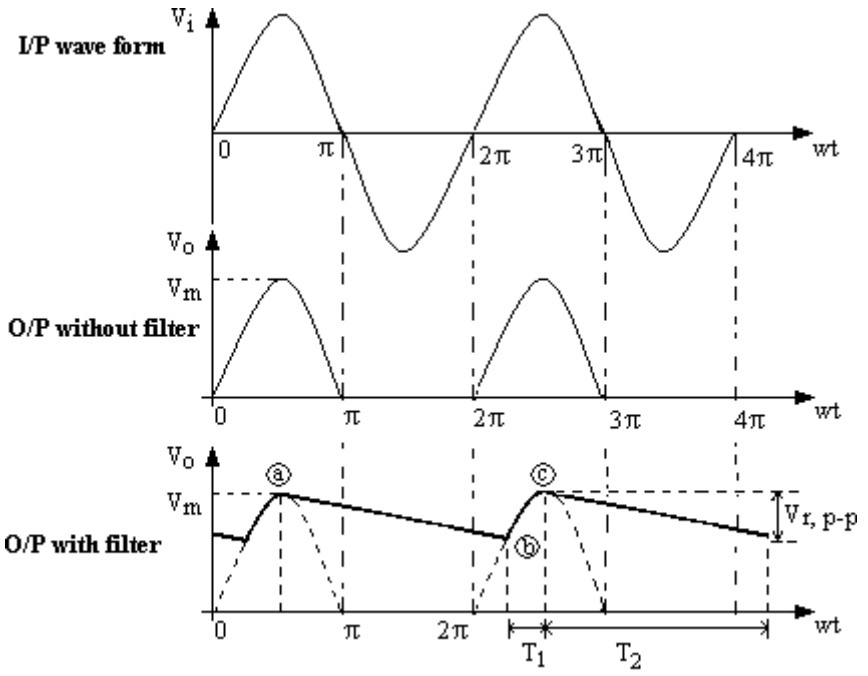



Half-wave Rectifier without filter




Half-wave Rectifier with capacitor filter

**WAVE SHAPES:**




Half-wave Rectifier with capacitor filter wave form

# 3. RECTIFIERS: HALF WAVE RECTIFIER

**Exp. No:…….** **Date:……**

**AIM:** To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Half wave rectifier with and without Capacitor filter.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Transformer | 230V / 0 - 9V | 1 |
| 2 | Diode | 1N4001 | 1 |
| 3 | Capacitors | 1000μF/16V, 470μf/25V | 1 |
| 4 | Decade Resistance Box | - | 1 |
| 5 | Multimeter | - | 1 |
| 6 | Bread Board and connecting wires | - | 1 Set |
| 7 | Dual Trace CRO | 20MHz | 1 |

**THEORY:**

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non zero average component is called a rectifier.

A practical half wave rectifier with a resistive load is shown in the circuit diagram. During the positive half cycle of the input the diode conducts and all the input voltage is dropped across $R_L$. During the negative half cycle the diode is reverse biased and it acts as almost open circuit so the output voltage is zero.

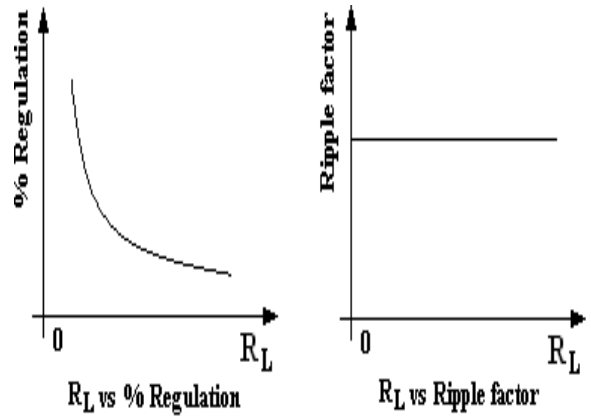
The filter is simply a capacitor connected from the rectifier output to ground. The capacitor quickly charges at the beginning of a cycle and slowly discharges through $R_L$ after the positive peak of the input voltage. The variation in the capacitor voltage due to charging and discharging is called ripple voltage. Generally, ripple is undesirable, thus the smaller the ripple, the better the filtering action.

**PROCEDURE:**

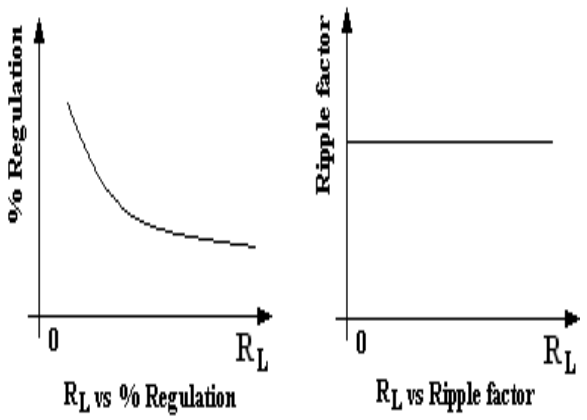
**WITHOUT FILTER**:

1. Connecting the circuit on bread board as per the circuit diagram
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the $R_L$ value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 1KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance ( DRB) and note down no load voltage Vdc ($V_{no\ load}$)

**MODEL GRAPHS:**




Without filter wave form




With filter wave form

6. Connect load resistance at 1KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
7. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of Regulation, $\%\eta = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} * 100\%$

**WITH CAPACITOR FILTER:**

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

**RESULT:** Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Half wave rectifier with and without filter.

**Without Filter:**

Ripple Factor :

Regulation :

**With Capacitor Filter:**

Ripple Factor :

Regulation :

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

**TABULAR FORMS:**

**WITHOUT FILTER:**

V no load Voltage (Vdc) = V

| S.No | Load Resistance $R_L$ (Ω) | O/P Voltage (Vo) | | Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$ | % of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$ |
|---|---|---|---|---|---|
| | | $V_{ac}$ (V) | $V_{dc}$ (V) | | |
| 1 | 100 | | | | |
| 2 | 200 | | | | |
| 3 | 300 | | | | |
| 4 | 400 | | | | |
| 5 | 500 | | | | |
| 6 | 600 | | | | |
| 7 | 700 | | | | |
| 8 | 800 | | | | |
| 9 | 900 | | | | |
| 10 | 1K | | | | |

**WITH CAPACITOR FILTER:**

V no load Voltage (Vdc) = V

| S.No | Load Resistance $R_L$ (Ω) | O/P Voltage (Vo) | | Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$ | % of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$ |
|---|---|---|---|---|---|
| | | $V_{ac}$ (V) | $V_{dc}$ (V) | | |
| 1 | 100 | | | | |
| 2 | 200 | | | | |
| 3 | 300 | | | | |
| 4 | 400 | | | | |
| 5 | 500 | | | | |
| 6 | 600 | | | | |
| 7 | 700 | | | | |
| 8 | 800 | | | | |
| 9 | 900 | | | | |
| 10 | 1K | | | | |

**VIVA QUESTIONS:**

1. What is a rectifier?

2. How Diode acts as a rectifier?

3. What is the significance of PIV? What is the condition imposed on PIV?

4. Draw the o/p wave form without filter?

5. Draw the o/p wave form with filter?

6. What is meant by ripple factor? For a good filter whether ripple factor should be high or low?

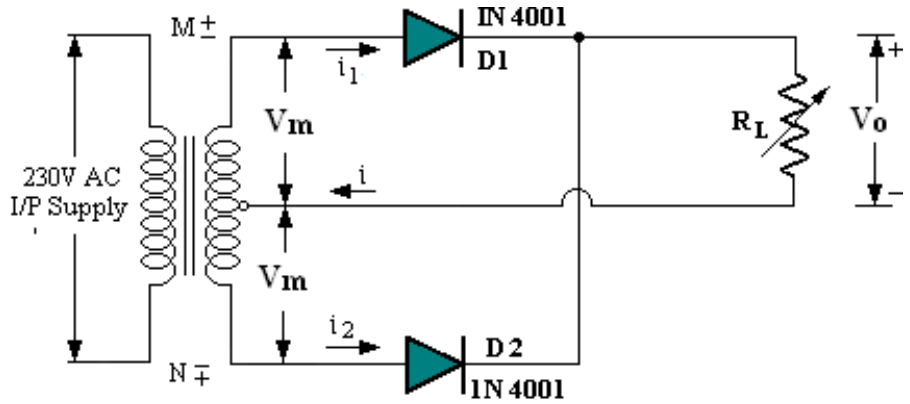
7. What is meant by regulation?

5. What is meant by time constant?

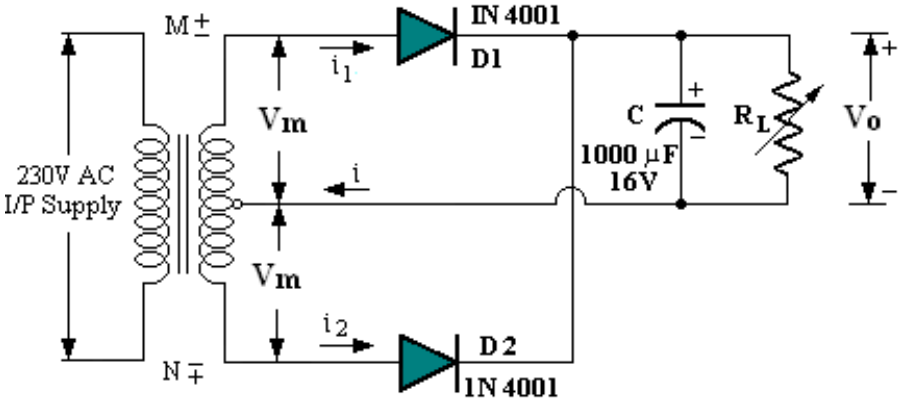
8. What happens to the o/p wave form if we increase the capacitor value?

9. What happens if we increase the capacitor value?

**CIRCUIT DIAGRAMS:**
**WITHOUT FILTER** AND **WITH FILTER:**

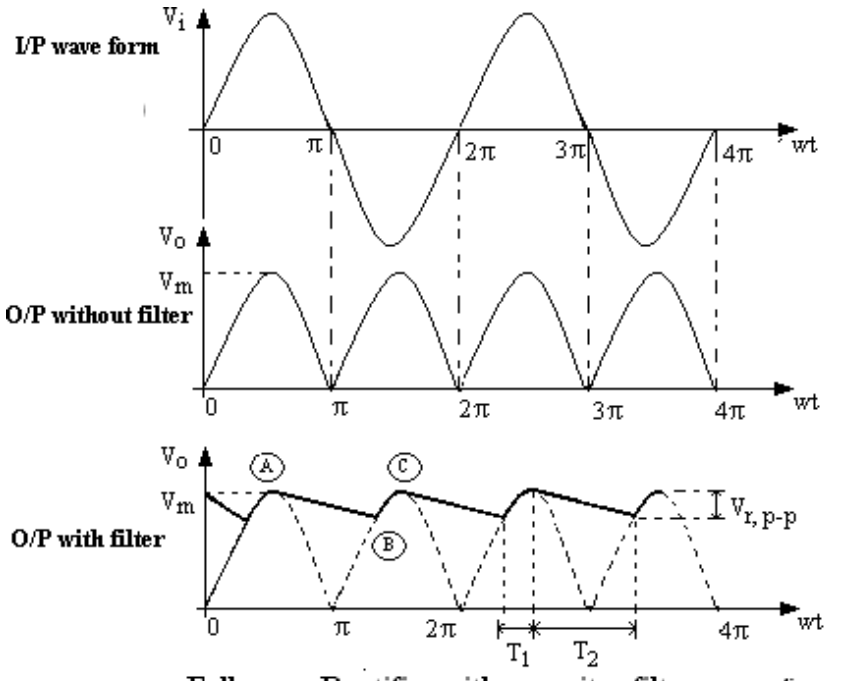



**Full-wave Rectifier without filter**




**Full-wave Rectifier with capacitor filter**

**WAVE SHAPES:**




**Full-wave Rectifier with capacitor filter wave form**

# 3. RECTIFIERS: FULL WAVE RECTIFIER

**Exp. No:…….** **Date:……**

**AIM:** To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full-wave rectifier center tapped circuit with and without Capacitor filter.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Transformer | 230V / 9-0-9V | 1 |
| 2 | Diode | 1N4001 | 2 |
| 3 | Capacitors | 1000μF/16V, 470μf/25V | 1 |
| 4 | Decade Resistance Box | - | 1 |
| 5 | Multimeter | - | 1 |
| 6 | Bread Board and connecting wires | - | 1 |
| 7 | Dual Trace CRO | 20MHz | 1 |

**THEORY:**

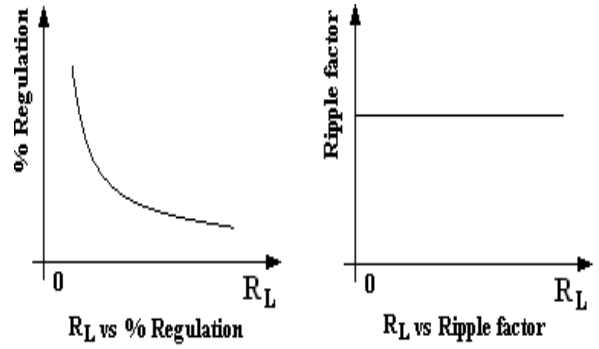
A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non zero average component is called a rectifier. A practical half wave rectifier with a resistive load is shown in the circuit diagram. It consists of two half wave rectifiers connected to a common load. One rectifies during positive half cycle of the input and the other rectifying the negative half cycle. The transformer supplies the two diodes (D1 and D2) with sinusoidal input voltages that are equal in magnitude but opposite in phase. During input positive half cycle, diode D1 is ON and diode D2 is OFF. During negative half cycle D1 is OFF and diode D2 is ON. Generally, ripple is undesirable, thus the smaller the ripple, the better the filtering action

**PROCEDURE:**

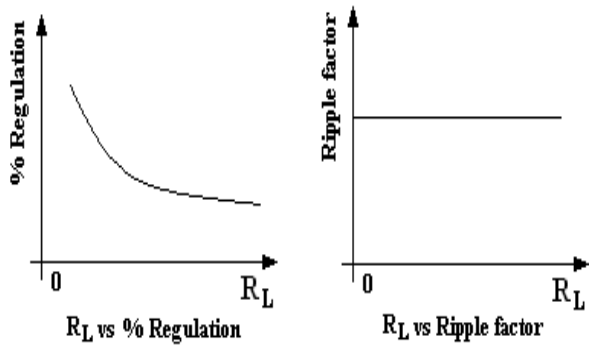
**WITHOUT FILTER**:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the $R_L$ value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 1KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance ( DRB) and note down no load voltage Vdc ($V_{no\ load}$)

**MODEL GRAPHS:**




Without filter wave form




With filter wave form

6. Connect load resistance at 1KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.

7. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$

8.Calculate Percentage of Regulation, $\%\eta = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} * 100\%$

**WITH CAPACITOR FILTER:**

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

**RESULT:** Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full-wave rectifier with and without filter.

**Without Filter:**

Ripple Factor :

Regulation :

**With Capacitor Filter:**

Ripple Factor :

Regulation :

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

**TABULAR FORMS:**

**WITHOUT FILTER:**

V no load Voltage (Vdc) = V

| S.No | Load Resistance $R_L$ (Ω) | O/P Voltage (Vo) | | Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$ | % of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$ |
|---|---|---|---|---|---|
| | | $V_{ac}$ (V) | $V_{dc}$ (V) | | |
| 1 | 100 | | | | |
| 2 | 200 | | | | |
| 3 | 300 | | | | |
| 4 | 400 | | | | |
| 5 | 500 | | | | |
| 6 | 600 | | | | |
| 7 | 700 | | | | |
| 8 | 800 | | | | |
| 9 | 900 | | | | |
| 10 | 1K | | | | |

**WITH CAPACITOR FILTER:**

V no load Voltage (Vdc) = V

| S.No | Load Resistance $R_L$ (Ω) | O/P Voltage (Vo) | | Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$ | % of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$ |
|---|---|---|---|---|---|
| | | $V_{ac}$ (V) | $V_{dc}$ (V) | | |
| 1 | 100 | | | | |
| 2 | 200 | | | | |
| 3 | 300 | | | | |
| 4 | 400 | | | | |
| 5 | 500 | | | | |
| 6 | 600 | | | | |
| 7 | 700 | | | | |
| 8 | 800 | | | | |
| 9 | 900 | | | | |
| 10 | 1K | | | | |

**VIVA QUESTIONS:**

1. What is a full wave rectifier?

2. How Diode acts as a rectifier?

3. What is the significance of PIV requirement of Diode in full-wave rectifier?

4. Compare capacitor filter with an inductor filter?

5. Draw the o/p wave form without filter? Draw the O/P? What is wave form with filter?

6. What is meant by ripple factor? For a good filter whether ripple factor should be high or low? What happens to the ripple factor if we insert the filter?

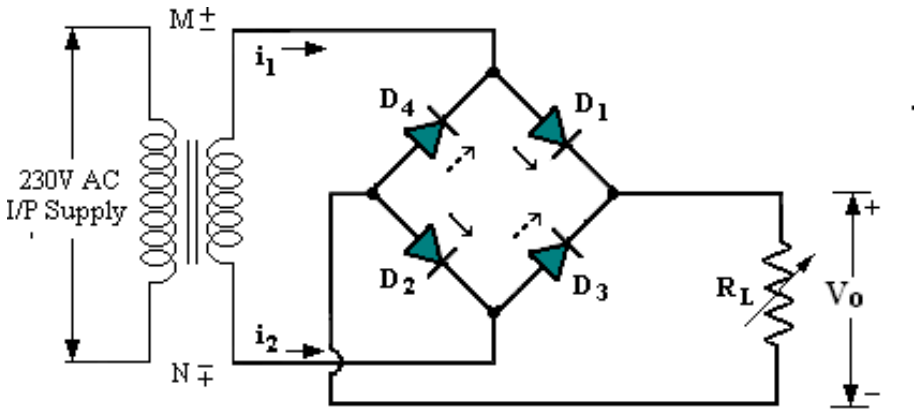
7. What is meant by regulation? Why regulation is poor in the case of inductor filter?

8. What is meant by time constant?

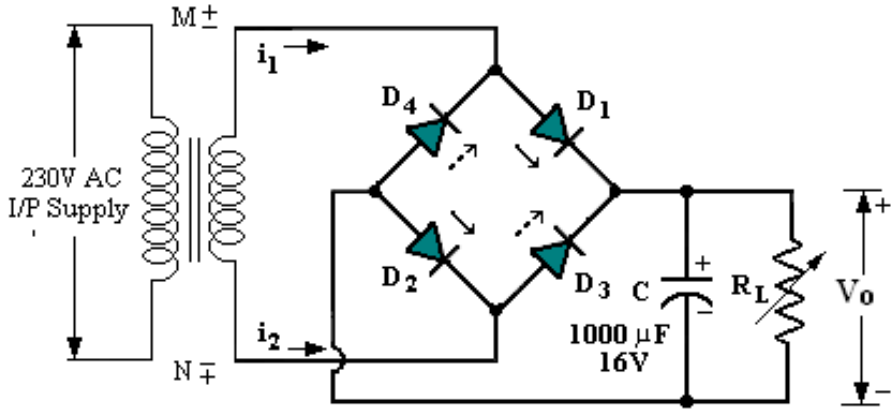
9. What happens to the o/p wave form if we increase the capacitor value? What happens if we increase the capacitor value?

10. What is the theoretical maximum value of ripple factor for a full wave rectifier?

**CIRCUIT DIAGRAMS:**
**WITH OUT FILTER & WITH FILTER:**

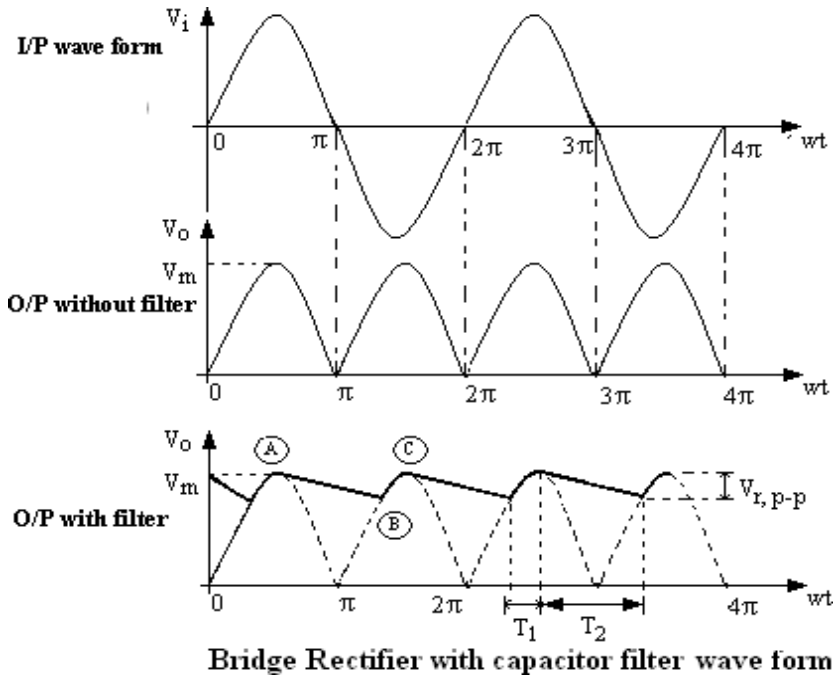



Bridge Rectifier without filter




Bridge Rectifier with capacitor filter

**WAVE SHAPES:**




Bridge Rectifier with capacitor filter wave form

# 3. RECTIFIERS: FULL WAVE BRIDGE RECTIFIER

**Exp. No:…….** **Date:……**

**AIM:** To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full-wave Bridge rectifier circuit with and without Capacitor filter.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Transformer | 230V / 0-9V | 1 |
| 2 | Diode | 1N4001 | 4 |
| 3 | Capacitors | 1000μF/16V, 470μf/25V | 1 |
| 4 | Decade Resistance Box | - | 1 |
| 5 | Multimeter | - | 1 |
| 6 | Bread Board and connecting wires | - | 1 |
| 7 | Dual Trace CRO | 20MHz | 1 |

**THEORY:**

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non zero average component is called a rectifier.

The Bridge rectifier is a circuit, which converts an ac voltage to dc voltage using both half cycles of the input ac voltage. The Bridge rectifier has four diodes connected to form a Bridge. The load resistance is connected between the other two ends of the bridge.

For the positive half cycle of the input ac voltage, diode D1 and D3 conducts whereas diodes D2 and D4 remain in the OFF state. The conducting diodes will be in series with the load resistance RL and hence the load current flows through $R_L$ .

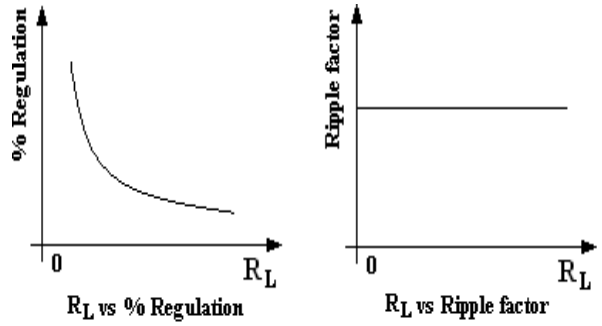
For the negative half cycle of the input ac voltage, diode D2 and D4 conducts whereas diodes D1 and D3 remain in the OFF state. The conducting diodes will be in series with the load resistance RL and hence the load current flows through RL in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave.

**PROCEDURE:**

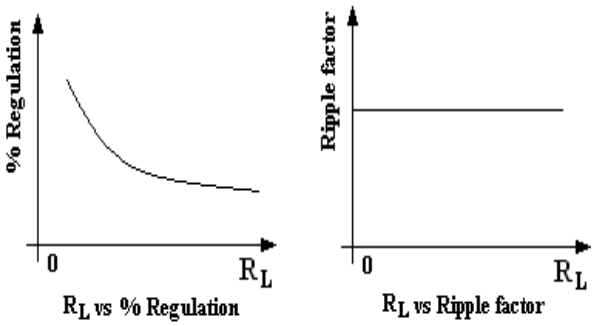
**WITHOUT FILTER**:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the $R_L$ value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 1KΩ and note down the Vac and Vdc as per given tabular form

**MODEL GRAPHS:**




Without filter wave form




With filter wave form

5. Disconnect load resistance ( DRB) and note down no load voltage Vdc ($V_{no\ load}$)
6. Connect load resistance at 1KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
7. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of Regulation, $\%\eta = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} * 100\%$

**WITH CAPACITOR FILTER:**

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

**RESULT:** Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full-wave Bridge rectifier with and without filter.

**Without Filter:**

Ripple Factor :

Regulation :

**With Capacitor Filter:**

Ripple Factor :

Regulation :

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

**TABULAR FORMS:**

**WITHOUT FILTER:**

V no load Voltage (Vdc) = V

| S.No | Load Resistance $R_L$ (Ω) | O/P Voltage (Vo) | | Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$ | % of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$ |
|---|---|---|---|---|---|
| | | $V_{ac}$ (V) | $V_{dc}$ (V) | | |
| 1 | 100 | | | | |
| 2 | 200 | | | | |
| 3 | 300 | | | | |
| 4 | 400 | | | | |
| 5 | 500 | | | | |
| 6 | 600 | | | | |
| 7 | 700 | | | | |
| 8 | 800 | | | | |
| 9 | 900 | | | | |
| 10 | 1K | | | | |

**WITH CAPACITOR FILTER:**

V no load Voltage (Vdc) = V

| S.No | Load Resistance $R_L$ (Ω) | O/P Voltage (Vo) | | Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$ | % of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$ |
|---|---|---|---|---|---|
| | | $V_{ac}$ (V) | $V_{dc}$ (V) | | |
| 1 | 100 | | | | |
| 2 | 200 | | | | |
| 3 | 300 | | | | |
| 4 | 400 | | | | |
| 5 | 500 | | | | |
| 6 | 600 | | | | |
| 7 | 700 | | | | |
| 8 | 800 | | | | |
| 9 | 900 | | | | |
| 10 | 1K | | | | |

**VIVA QUESTIONS:**

1. What are the advantages of Bridge Rectifier over the center tapped Rectifier?

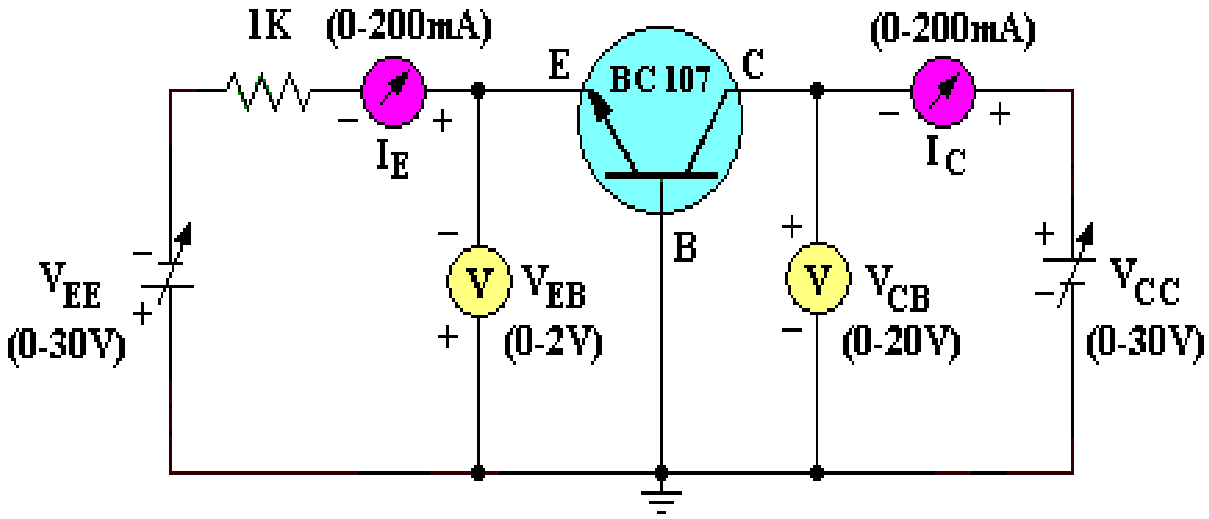
2. What does Regulation indicate?

3. What is the Theoretical maximum value of Ripple factor of a Full-wave Rectifier?

4. What is the PIV requirement of a Diode in a Bridge Rectifier?

5. Explain the operation of Bridge Rectifier?

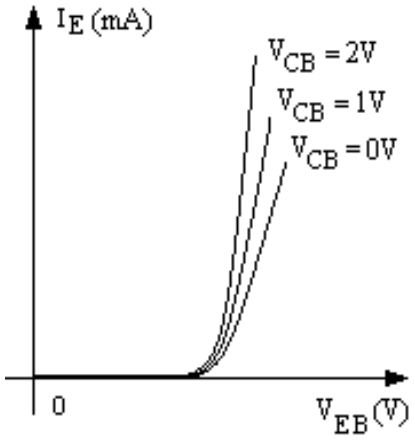
**CIRCUIT DIAGRAMS:**



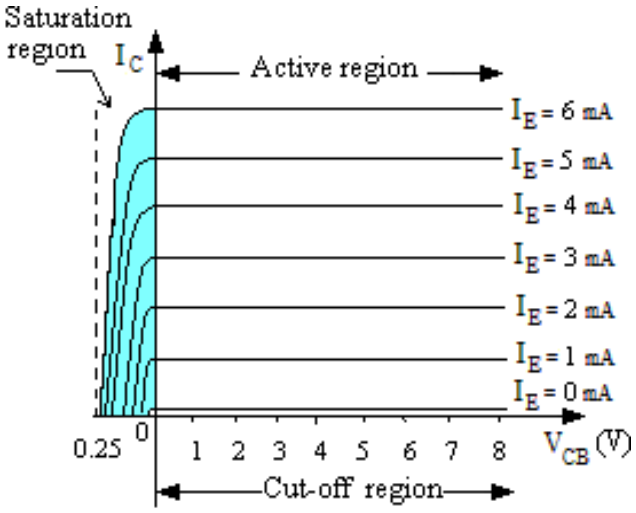

**Common Base Transistor Characteristics**

**MODEL GRAPHS;**

1. Plot the Input characteristics by taking $I_E$ on y–axis and $V_{EB}$ on x–axis.
2. Plot the Output characteristics by taking $I_C$ on y–axis and $V_{CB}$ on x–axis.




**CB I/P Characteristics**




**CB O/P Characteristics**

# 4. BJT CHARACTERISTICS (CB)

**Exp. No:…….** **Date:……**

**AIM:** To plot the Input and Output characteristics of a transistor connected in Common Base Configuration and to find the h – parameters from the characteristics.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Dual Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | Transistor | BC107 | 1 |
| 3 | Resistors | 1KΩ | 1 |
| 4 | DC Ammeters | (0-200mA) | 2 |
| 5 | DC Voltmeters | (0-2V), (0-20V) | Each 1 No |
| 6 | Bread Board and connecting wires | - | 1 Set |

**THEORY:**

Bipolar junction transistor (BJT) is a 3 terminal (emitter, base, collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely emitter junction and collector junction.

In Common Base configuration the input is applied between emitter and base and the output is taken from collector and base. Here base is common to both input and output and hence the name common base configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between $V_{EB}$ and $I_E$ at constant $V_{CB}$ in CB configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between $V_{CB}$ and $I_C$ at constant $I_E$ in CB configuration.

**PROCEDURE:**
**TO FIND THE INPUT CHARACTERISTICS:**

1. Connect the circuit as in the circuit diagram.
2. Keep $V_{EE}$ and $V_{CC}$ in zero volts before giving the supply
3. Set $V_{CB}$ = 1 volt by varying $V_{CC}$. and vary the $V_{EE}$ smoothly with fine control such that emitter current $I_E$ varies in steps of 0.2mA from zero upto 20mA, and note down the corresponding voltage $V_{EB}$ for each step in the tabular form.
4. Repeat the experiment for $V_{CB}$ =2 volts and 3 volts.
5. 
6. Draw a graph between $V_{EB}$ Vs $I_E$ against $V_{CB}$ = Constant.

**TO FIND THE OUTPUT CHARACTERISTICS:**

1. Start $V_{EE}$ and $V_{CC}$ from zero Volts.
2. Set the $I_E$ = 1mA by using $V_{EE}$ such that, $V_{CB}$ changes in steps of 1.0 volts from zero upto 20 volts, note down the corresponding collector current $I_C$ for each step in the tabular form.
3. Repeat the experiment for $I_E$ = 3mA and $I_E$ = 5mA, tabulate the readings.
4. Draw a graph between $V_{CB}$ Vs $I_C$ against $I_E$ = Constant.

**To find the h – parameters:**

**Calculation of hib:**

Mark two points on the Input characteristics for constant $V_{CB}$. Let the coordinates of these two points be ($V_{EB1}$, $I_{E1}$) and ($V_{EB2}$, $I_{E2}$).

$$h_{ib} = \frac{V_{EB2} - V_{EB1}}{I_{E2} - I_{E1}};$$

**Calculation of hrb:**

Draw a horizontal line at some constant $I_E$ value on the input characteristics. Find $V_{CB2}$, $V_{CB1}$, $V_{EB2}$, $V_{EB1}$

$$h_{rb} = \frac{V_{EB2} - V_{EB1}}{V_{CB2} - V_{CB1}};$$

**Calculation of hfb:**

Draw a vertical line on the Output characteristics at some constant $V_{CB}$ value. Find $I_{c2}$, $I_{c1}$ and $I_{E2}$, $I_{E1}$ .

$$h_{fb} = \frac{I_{C2} - I_{C1}}{I_{E2} - I_{E1}};$$

**Calculation of hob:**

On the Output characteristics for a constant value of $I_E$ mark two points with coordinates ($V_{CB2}$ , $I_{C2}$) and ($V_{CB1}$ , $I_{C1}$) .

$$h_{ob} = \frac{I_{C2} - I_{C1}}{V_{CB2} - V_{CB1}};$$

**RESULTS:**

The Input and Output characteristics are drawn on the graphs and the h parameters are calculated .

$h_{ib}$= --------- ohms. $h_{rb}$= ----------

$h_{ob}$= -------- mhos. $h_{fb}$ = ----------

**TABULAR FORMS:**

**INPUT CHARACTERISTICS;**

| S.No | $V_{CB}$ = 0V | | $V_{CB}$ = 1V | | $V_{CB}$ = 2V | |
|---|---|---|---|---|---|---|
| | $V_{EB}$ (V) | $I_E$ (mA) | $V_{EB}$ (V) | $I_E$ (mA) | $V_{EB}$ (V) | $I_E$ (mA) |
| 1 | | 0.0 | | 0.0 | | 0.0 |
| 2 | | 0.2 | | 0.2 | | 0.2 |
| 3 | | 0.4 | | 0.4 | | 0.4 |
| 4 | | 0.6 | | 0.6 | | 0.6 |
| 5 | | 0.8 | | 0.8 | | 0.8 |
| 6 | | 1.0 | | 1.0 | | 1.0 |
| 7 | | 4.0 | | 4.0 | | 4.0 |
| 8 | | 8.0 | | 8.0 | | 8.0 |
| 9 | | 10.0 | | 10.0 | | 10.0 |
| 10 | | 14.0 | | 14.0 | | 14.0 |
| 11 | | 18.0 | | 18.0 | | 18.0 |
| 12 | | 20.0 | | 20.0 | | 20.0 |

**OUTPUT CHARACTERISTICS;**

| S.No | $I_E$ = 1 mA | | $I_E$ = 3 mA | | $I_E$ = 5 mA | |
|---|---|---|---|---|---|---|
| | $V_{CB}$ (V) | $I_C$ (mA) | $V_{CB}$ (V) | $I_C$ (mA) | $V_{CB}$ (V) | $I_C$ (mA) |
| 1 | 0.0 | | | 0.0 | | 0.0 |
| 2 | 0.2 | | | 0.2 | | 0.2 |
| 3 | 0.4 | | | 0.4 | | 0.4 |
| 4 | 0.6 | | | 0.6 | | 0.6 |
| 5 | 0.8 | | | 0.8 | | 0.8 |
| 6 | 1.0 | | | 1.0 | | 1.0 |
| 7 | 3.0 | | | 3.0 | | 3.0 |
| 8 | 5.0 | | | 5.0 | | 5.0 |
| 9 | 7.0 | | | 7.0 | | 7.0 |
| 10 | 10.0 | | | 10.0 | | 10.0 |
| 11 | 12.0 | | | 12.0 | | 12.0 |
| 12 | 15.0 | | | 15.0 | | 15.0 |

**VIVA QUESTION:**

1. What is Early effect?

2. Draw the small signal model of BJT Common Base Configuration.

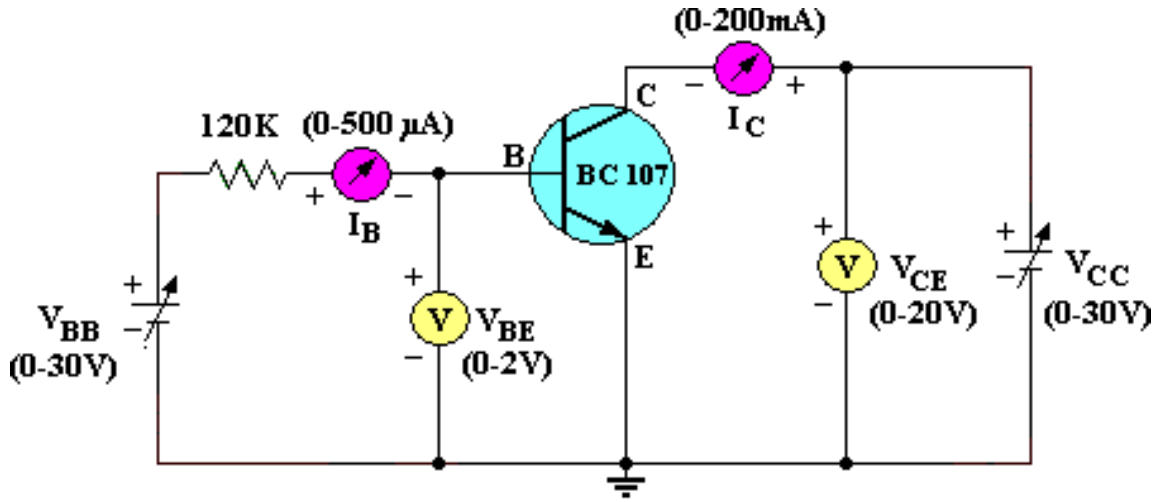
3. What is Reach –Through effect?

4. What are the applications of Common Base.

5. What will be the parameters of CB.

6. Explain the Transistor operation?

**CIRCUIT DIAGRAMS:**

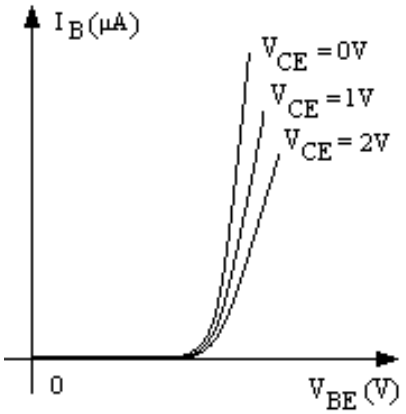



**Common Emitter Transistor Characteristics**

**MODEL GRAPHS:**

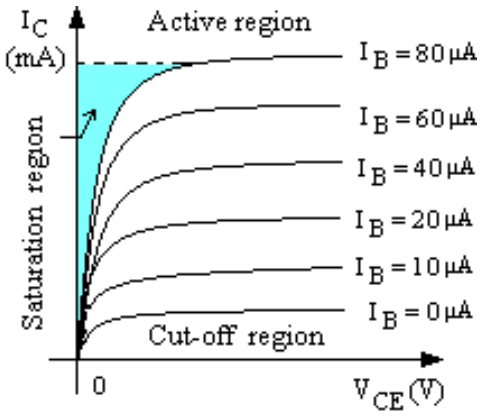
1. Plot the Input characteristics by taking $I_B$ on y-axis and $V_{BE}$ on x-axis.
2. Plot the Output characteristics by taking $I_C$ on the y-axis and $V_{CE}$ on x-axis.

**INPUT CHARACTERISTICS:**




**CE I/P Characteristics**

**OUTPUT CHARACTERISTICS:**




**CE O/P Characteristics**

# 4. BJT CHARACTERISTICS (CE)

**Exp. No:…….** **Date:……**

**AIM:** To plot the Input and Output characteristics of a transistor connected in Common Emitter Configuration and to find the h – parameters from the characteristics.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Dual Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | Transistor | BC107 | 1 |
| 3 | Resistors | 120KΩ | 1 |
| 4 | DC Ammeters | (0-500μA), (0-200mA) | Each 1 No |
| 5 | DC Voltmeters | (0-2V), (0-20V) | Each 1 No |
| 6 | Bread Board and connecting wires | - | 1 Set |

**THEORY:**

Bipolar junction transistor (BJT) is a 3 terminal (emitter, base, collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely emitter junction and collector junction.

In Common Emitter configuration the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between $V_{BE}$ and $I_B$ at constant $V_{CE}$ in CE configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between $V_{CE}$ and $I_C$ at constant $I_B$ in CE configuration.

**PROCEDURE:**

**TO FIND THE INPUT CHARACTERISTICS:**

1. Connect the circuit as in the circuit diagram.
2. Keep $V_{BB}$ and $V_{CC}$ in zero volts before giving the supply
3. Set $V_{CE}$ = 1 volt by varying $V_{CC}$ and vary the $V_{BB}$ smoothly with fine control such that base current $I_B$ varies in steps of 5μA from zero upto 200μA, and note down the corresponding voltage $V_{BE}$ for each step in the tabular form.

4. Repeat the experiment for $V_{CE}$ =2 volts and 3 volts.
5. Draw a graph between $V_{BE}$ Vs $I_B$ against $V_{CE}$ = Constant.

**TO FIND THE OUTPUT CHARACTERISTICS:**

1. Start $V_{EE}$ and $V_{CC}$ from zero Volts.
2. Set the $I_B$ = 20μA by using $V_{BB}$ such that, $V_{CE}$ changes in steps of 0.2 volts from zero upto 10 volts, note down the corresponding collector current $I_C$ for each step in the tabular form.
3. Repeat the experiment for $I_E$ = 40μA and $I_E$ = 60μA, tabulate the readings.
4. Draw a graph between $V_{CE}$ Vs $I_C$ against $I_B$ = Constant.

**To find the h – parameters:**

**Calculation of $h_{ie}$:**

Mark two points on the Input characteristics for constant $V_{CE}$. Let the coordinates of these two points be ($V_{BE1,}$ $I_{B1}$) and ($V_{BE2,}$ $I_{B2}$).

$$h_{ie} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}};$$

**Calculation of $h_{re}$:**

Draw a horizontal line at some constant $I_B$ value on the Input characteristics. Find $V_{CE2}$, $V_{CE1}$, $V_{BE2}$, $V_{BE1}$

$$h_{re} = \frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}};$$

**Calculation of $h_{fe}$:**

Draw a vertical line on the out put characteristics at some constant $V_{CE}$ value. Find $Ic_{2,}$ $Ic_1$ and $I_{B2,}$ $I_{B1}$ .

$$h_{fe} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}};$$

**Calculation of $h_{oe}$:**

On the Output characteristics for a constant value of $I_B$ mark two points with coordinates ($V_{CE2}$ , $I_{C2}$) and ($V_{CE1}$ , $I_{C1}$) .

$$h_{oe} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}};$$

**RESULTS:**

The input and out put characteristics are drawn on the graphs and the h parameters are calculated .

hie= --------- ohms. hre= ---------- hoe= -------- mhos. hfe = ----------

**TABULAR FORMS:**

**INPUT CHARACTERISTICS;**

| S.No | $V_{CE}$ = 0V | | $V_{CE}$ = 1V | | $V_{CE}$ = 2V | |
|---|---|---|---|---|---|---|
| | $V_{BE}$ (V) | $I_B$ (µA) | $V_{BE}$ (V) | $I_B$ (µA) | $V_{BE}$ (V) | $I_B$ (µA) |
| 1 | | 0 | | 0 | | 0 |
| 2 | | 5 | | 5 | | 5 |
| 3 | | 10 | | 10 | | 10 |
| 4 | | 20 | | 20 | | 20 |
| 5 | | 40 | | 40 | | 40 |
| 6 | | 60 | | 60 | | 60 |
| 7 | | 80 | | 80 | | 80 |
| 8 | | 100 | | 100 | | 100 |
| 9 | | 120 | | 120 | | 120 |
| 10 | | 140 | | 140 | | 140 |
| 11 | | 180 | | 180 | | 180 |
| 12 | | 200 | | 200 | | 200 |

**OUTPUT CHARACTERISTICS;**

| S.No | $I_B$ = 20 µA | | $I_B$ = 40 µA | | $I_B$ = 60 µA | |
|---|---|---|---|---|---|---|
| | $V_{CE}$ (V) | $I_C$ (mA) | $V_{CE}$ (V) | $I_C$ (mA) | $V_{CE}$ (V) | $I_C$ (mA) |
| 1 | 0.0 | | 0.0 | | 0.0 | |
| 2 | 0.2 | | 0.2 | | 0.2 | |
| 3 | 0.4 | | 0.4 | | 0.4 | |
| 4 | 0.6 | | 0.6 | | 0.6 | |
| 5 | 0.8 | | 0.8 | | 0.8 | |
| 6 | 1.0 | | 1.0 | | 1.0 | |
| 7 | 3.0 | | 3.0 | | 3.0 | |
| 8 | 5.0 | | 5.0 | | 5.0 | |
| 9 | 7.0 | | 7.0 | | 7.0 | |
| 10 | 10.0 | | 10.0 | | 10.0 | |

**VIVA QUESTION:**

1. Why CE configuration is most widely used?

2. Draw the equivalent Circuit of C.E

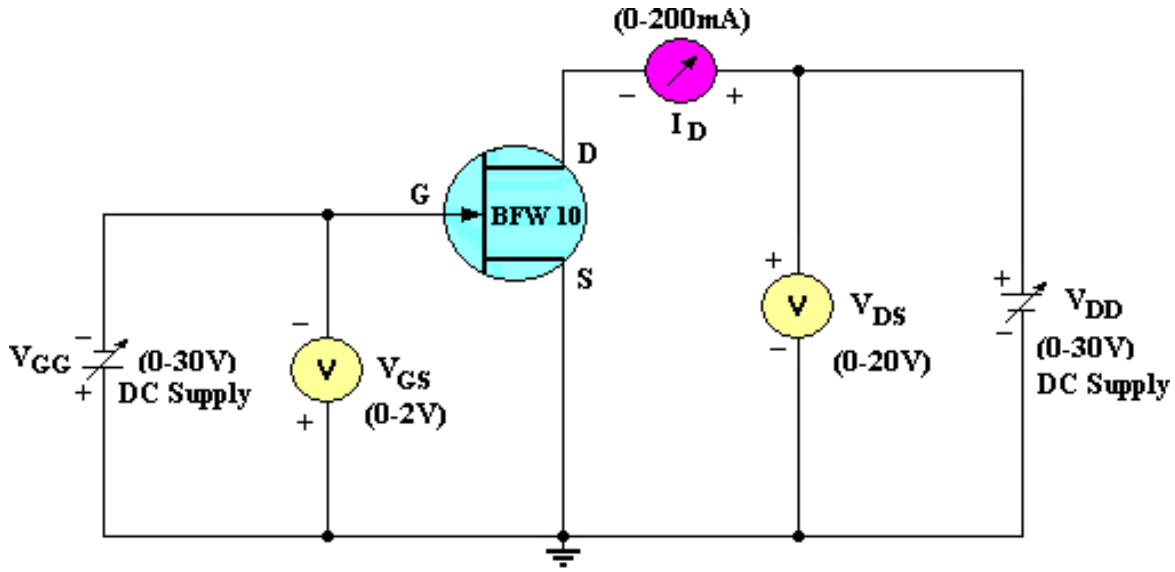
3. What is the Current Gain,voltage gain,i/p and o/p impedance in CE?.

4. Relation between „α" and „β" and γ

5. Give the condition to operate the given Transistor in active,saturation &Cut-off Regions

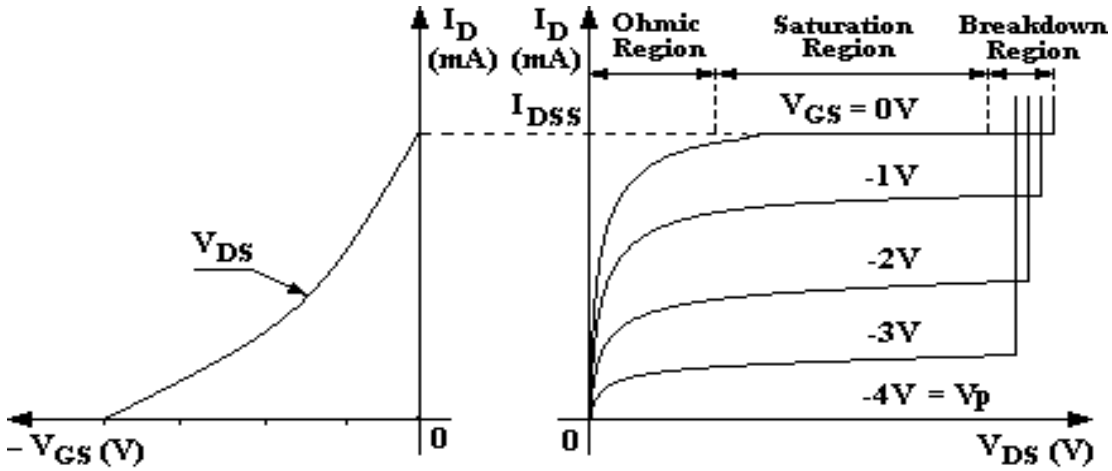
What is Emitter Efficiency

**CIRCUIT DIAGRAM:**




JFET Drain Characteristics

**MODEL GRAPH:**




FET Transfer Characteristics

FET Drain Characteristics

# 5. FET CHARACTERISTICS (CS Configuration)

**Exp. No:…….** **Date:……**

**AIM:**

To conduct an experiment on a given JFET and obtain

1) Drain characteristics
2) Transfer Characteristics.
3) To find $r_d$, $g_m$, and $\mu$ from the characteristics.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Dual Regulated D.C Power supply | (0–30 Volts) | 1 |
| 2 | JFET | BFW 10 or 11 | 1 |
| 3 | D.C Ammeter | (0 – 20mA) | 1 |
| 4 | D.C Voltmeters | (0 – 2V), (0 – 20V) | Each 1 |
| 5 | Bread Board and connecting wires | -- | 1 Set |

**THEORY:**

## Introduction:


The field effect transistor (FET) is made of a bar of N type material called the SUBSTRATE with a P type junction (the gate) diffused into it. With a positive voltage on the drain, with respect to the source, electron current flows from source to drain through the CHANNEL.

If the gate is made negative with respect to the source, an electrostatic field is created which squeezes the channel and reduces the current. If the gate voltage is high enough the channel will be "pinched off" and the current will be zero. The FET is voltage controlled, unlike the transistor which is current controlled. This device is sometimes called the junction FET or IGFET or JFET.

If the FET is accidentally forward biased, gate current will flow and the FET will be destroyed. To avoid this, an extremely thin insulating layer of silicon oxide is placed between the gate and the channel and the device is then known as an insulated gate FET, or IGFET or

metal oxide semiconductor FET (MOSFET) Drain characteristics are obtained between the drain to source voltage ($V_{DS}$) and drain current ($I_D$) taking gate to source voltage ($V_{GS}$) as the parameter. Transfer characteristics are obtained between the gate to source voltage ($V_{GS}$) and Drain current ($I_D$) taking drain to source voltage ($V_{DS}$) as parameter

**PROCEDURE:**

**DRAIN CHARACTERISTICS:**

1. Connect the circuit as per the Fig. 1 and start with $V_{GG}$ and $V_{DD}$ keeping at zero volts.
2. Keep $V_{GG}$ such that $V_{GS}$ = 0 volts, Now vary $V_{DD}$ such that $V_{DS}$ Varies in steps of 1 volt up to 10 volts. And Note down the corresponding Drain current $I_D$
3. Repeat the above experiment with $V_{GS}$ = -1V and -2V and tabulate the readings.
4. Draw a graph $V_{DS}$ Vs $I_D$ against $V_{GS}$ as parameter on graph.
5. From the above graph calculate $r_d$ and note down the corresponding diode current against the voltage in the tabular form.
6. Draw the graph between voltage across the Diode Vs Current through the diode in the first quadrant as shown in fig.

**TRANSFER CHARACTERISTICS:**

1. Set $V_{GG}$ and $V_{DD}$ at zero volts .keep $V_{DS}$ = 1Volt.
2. Vary $V_{GG}$ such that $V_{GS}$ varies in steps of 0.5 volts. Note down the corresponding Drain current $I_D$, until $I_D$ = 0mA and Tabulate the readings.
3. Repeat the above experiment for $V_{DS}$ = 3.0 Volts and 5.0 Volts and tabulate the readings.
4. Draw graph between $V_{GS}$ Vs $I_D$ with $V_{DS}$ as parameter.
5. From the graph find $g_m$.
6. Now $\mu = g_m \times r_d$.

**TABULAR FORM:**

**DRAIN CHARACTERISTICS:**

| S.No | | $V_{GS}$ = 0 volts | $V_{GS}$ = -1V | $V_{GS}$ = -2V |
|---|---|---|---|---|
| | $V_{DS}$ (V) | $I_D$ (mA) | $I_D$ (mA) | $I_D$ (mA) |
| 1 | 0.0 | | | |
| 2 | 0.5 | | | |
| 3 | 1.0 | | | |
| 4 | 1.5 | | | |
| 5 | 2.0 | | | |
| 6 | 2.5 | | | |
| 7 | 3.0 | | | |
| 8 | 3.5 | | | |
| 9 | 4.0 | | | |
| 10 | 4.5 | | | |
| 11 | 5.0 | | | |
| 12 | 5.5 | | | |
| 13 | 6.0 | | | |

**TRANSFER CHARACTERISTICS:**

| S.No | | $V_{DS}$ = 1.0V | $V_{DS}$ = 3.0V | $V_{DS}$ = 5.0V |
|---|---|---|---|---|
| | $V_{GS}$ (V) | $I_D$ (mA) | $I_D$ (mA) | $I_D$ (mA) |
| 1 | 0.0 | | | |
| 2 | 0.5 | | | |
| 3 | 1.0 | | | |
| 4 | 1.5 | | | |
| 5 | 2.0 | | | |

**CALCULATIONS:**

**CALCULATION OF $r_d$ :**

Construct a Triangle on one of the output characteristic for a particular $V_{GS}$ in the active region and find $\Delta V_{DS}$ and $\Delta I_D$

Now $\mathbf{r_d} = \Delta V_{DS} / \Delta I_D$ ($V_{GS}$ = constant)

**CALCULATION OF $g_m$ :**

Construct a Triangle on one of the Transfer characteristics for a particular $V_{DS}$ find $\Delta V_{GS}$ and $\Delta I_D$.

Now $\mathbf{g_m} = \Delta I_D / \Delta V_{GS}$ ($V_{DS}$ = constant).

**CALCULATION OF $\mu$ :**

$$\mu = g_m \times r_d.$$

**RESULT:**

**PRECAUTIONS:**

1. check the wires for continuity before use.
2. keep the power supply at zero volts before starting the experiment.
3. All the contacts must be intact.
4. For a good JFET $I_D$ will be $\geq$ 11.0 mA at $V_{GS}$ = 0.0 volts if not change the JFET.

**VIVA QUESTIONS:**

1. What are the advantages of JFET over BJT?

2. Why input resistance in FET amplifier is more than the BJT amplifier?

3. What is a uni-polar device?

4. What is pinch off voltage?

5. What are various FETs?

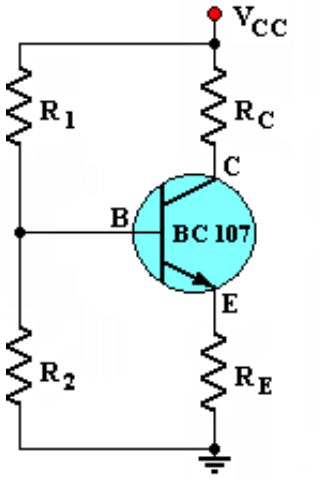
6. What is Enhancement mode and Depletion mode?

7. Draw the Equivalent circuit of JFET for low frequencies?

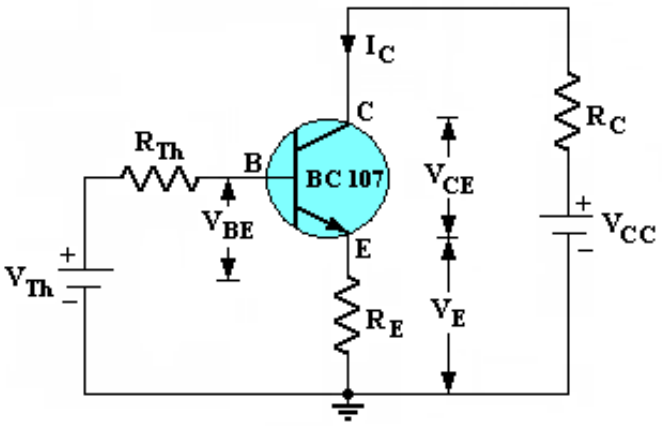
8. Write the mathematical equation for $g_m$ in terms of $g_{mo}$?

9. Write equation of FET $I_D$ in terms of $V_{GS}$ and $V_p$?

**CIRCUIT DIAGRAMS:**




Self Bias circuit




Self Bias equivalent circuit

**DESIGN PROCEDURE:**

Icq = 5mA, Vceq = 6.0 V, Vcc = 12.0 V, Rc = 1K, S = 25,Vbe=0.6 V.

Find hfe of the transistor

$S= (1+\beta) / (1+\beta Re / (Re + Rb))$

$V_B = V_{CC}R_2 / (R_1 + R_2)$

$R_B = R_1R_2 / (R_1+R_2)$

$V_B = I_BR_B + V_{BE} + (1+\beta)I_BR_E$

$V_{CC} = I_CR_C + V_{CE} + (1+\beta)I_BR_E$, & $Ic=\beta I_B$

Using the above formula find Re, R1, R2.

## 6. TRANSISTOR BIASING - Design Self Bias Circuit

**Exp. No:…….** **Date:……**

**AIM:** Design a Self Bias Circuit For the following Specifications
$h_{fe}$ = , Icq = 5mA, Vceq = 6.0 V, Vcc = 12.0 V, Rc = 1KΩ, S = 25.

Find the quiescent point (Operating Point) values of $I_{CQ}$ and $V_{CE}q$ from the experiment and to find the maximum signal handling capability of the Amplifier.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Dual Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | Transistor | BC107 | 1 |
| 3 | Capacitors | 50μf | 2 |
| 4 | Capacitors | 10μf | 1 |
| 5 | Multimeter | - | 1 |
| 6 | Signal Generator | ( 0 – 1MHz) | 1 |
| 7 | Bread Board and connecting wires | - | 1 Set |
| 8 | Dual Trace CRO | 20MHz | 1 |

**THEORY:**

The collector to base feedback configuration ensures that the transistor is always biased in the active region regardless of the value of Beta (β) as the base bias is derived from the collector voltage.

In this circuit, the base bias resistor, RB is connected to the transistors collector C, instead of to the supply voltage, Vcc. Now if the collector current increases, the collector voltage drops, reducing the base drive and thereby automatically reducing the collector current. Therefore the network balances itself. That is why this method of negative feedback biasing is called self-biasing

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram. Apply Vcc of 12 Volts DC.
2. Find the resulting DC Values of Icq and Vceq.
3. Apply a 1KHz signal from the Signal Generator and observe the O/P on CRO.
4. Increase the I/P voltage slowly until the output waveform starts distortion
5. Note down the input voltage Vi at the point where the output starts distortion
6. This input value is known as maximum signal handling capability.
7. Calculate the gain of the amplifier.

**TABULAR FORM:**

| Parameter | Theoretical Values | Practical ValuesName |
|---|---|---|
| $I_C$ | | |
| $V_{CE}$ | | |
| $R_1$ | | |
| $R_2$ | | |
| $R_E$ | | |
| $R_B$ | | |

**RESULT:**

The maximum signal Handling capability of the amplifier = Volts

Gain of the amplifier =

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start
3. All the contacts must be intact

**VIVA QUESTIONS:**

1. What is meant by Self Bias & fixed Bias circuits, Which one is preferred and why?

2. What is the significance of Emitter Resistance?

4. What is stability factor?

5. what is DC Load line and A.C. Load line?

6. what is quiescent point? What are the various parameters of the transistor that cause drift in q-point?

7. what are different techniques of stabilization?

8. Relate stability factor with the circuit parameters

9. What is the relation between $\alpha$ and $\beta$.

10. If bypass capacitor is removed ,what happens to the gain?

# 7. CRO OPERATIONS AND ITS MEASUREMENTS

**Exp. No:…….** **Date:……**

**AIM:** To Study of C.R.O. Voltage measurement on C.R.O. Current measurement on C.R.O. Frequency measurement on C.R.O. Phase difference measurement on C.R.O.

**APPARATUS REQUIRED:** Cathode-ray oscilloscope, Function Generator.

**THEORY:**


**Front Panel Controls of CRO:**

| | | |
|---|---|---|
| 1. | POWER ON | Put the instrument to main supply with LED indication. |
| 2. | INTENSITY | Controls the brightness of the display. |
| 3. | FOCUS | Controls the sharpness of the display |
| 4. | TIME BASE | 18 step switch to enable selection of 18 calibrated sweep from 0.5 micro sec/div to0.2s/div in 1,2,5,….sequence |
| 5. | TIME BASE VARIABLE | In calibrated position(CAL)the selected sweep speed holds indicated calibration clockwise. It extends the sweep speed by 2.5 times approx. with the LED indication. |
| 6. | HOLD-OFF | Provides 4:1 Hold off to enhance HF &Complex Signal Triggering. |
| 7. | ⇔ POSITION/x5 | Controls the horizontal position of the display. When this control is pulled, it magnifies the sweep 5 times with LED indication. |
| 8. | LEVEL | Variable control, selects the trigger point on the displayed waveform. |
| 9. | AUTO/NORM | In auto mode trace is displayed in absence of any input signal. The display is then automatically triggered for signals above 30 Hz depending upon correct setting of trigger LEVEL controls. |

| | | |
|---|---|---|
| 10. | INT/EXT | INT; Display triggers from signals derived from CH1, CH2 or line.EXT: triggering from any other external source fed through EXT TRIG BNC socket. |
| 11. | LINE | Triggers from power line frequency. |
| 12. | TV | Triggers from low freq. component of TV signal (TV-V or TV-H). |
| 13. | +/- | Selects trigger point on either positive or negative slope of the displayed waveform. |
| 14. | CH1/CH2 | Select trigger signal in INT mode derived from either CH1 or CH2 inputs. |
| 15. | HF Rej | Introduces low pass filter (20 KHz) in trigger. |
| 16. | ac/dc | Selects trigger signal coupling. |
| 17. | SWP/X-Y | When pressed, converts CH2 input into x-channel and enable use of the scope as on X-Y scope (Y-input via. CH1). In released position, SWEEP operates. |
| 18. | 0.2, 1KHz | 200 mv p-p 1 KHz square wave calibration signal. |
| 19. | ⇳ Positions | Controls the vertical position of the display |
| 20. | ac/dc/gnd | Selects input coupling / grounding (Grounds the amplifier input but input signal is open circuited) |
| 21. | EXT-TRIG | Input BNC for external trigger signal |
| 22. | INPUT BNC CH1/Y (CH2/X) | Input terminals to CH1/Y, CH2/X inputs |
| 23. | TRACE | Screw driver control to adjust horizontal tilt of the trace. |
| 24. | CH1/CH2 ATTENUATOR | 12 steps compensated attenuator from 5 mv/div to 20 V/div in 1,2,5 sequence. |
| 25. | VERTICAL MODES | |
| | a. ALT/CHOP | Selects switching mode for 2 channel while in DUAL operations |
| | b. DUAL/MONO (X-Y) | In DUAL, operates as a DUAL trace scope in ALT or CHOP mode as selected. |
| | c. CHANNEL ADDTION (CH1-CH2) | In DUAL mode, when ADD switch is pressed signals of CH1 and CH2 are algebraically added. |
| | d. CHANNEL SUBRACTION (CH1-CH2) | In DUAL mode, when ADD and CH2 INV switches are pressed CH2 signal is algebraically subtracted from CH1 signal. |
| | e. CH2 INV | When CH2 INV switch is pressed polarity of the signal to CH2 is inverted. |
| | | |

**About CRO:**

The cathode-ray oscilloscope (CRO) is a common laboratory instrument that provides accurate time and amplitude measurements of voltage signals over a wide range of frequencies. Its reliability, stability, and ease of operation make it suitable as a general purpose laboratory instrument. The heart of the CRO is a cathode-ray tube shown schematically in Fig. 1.

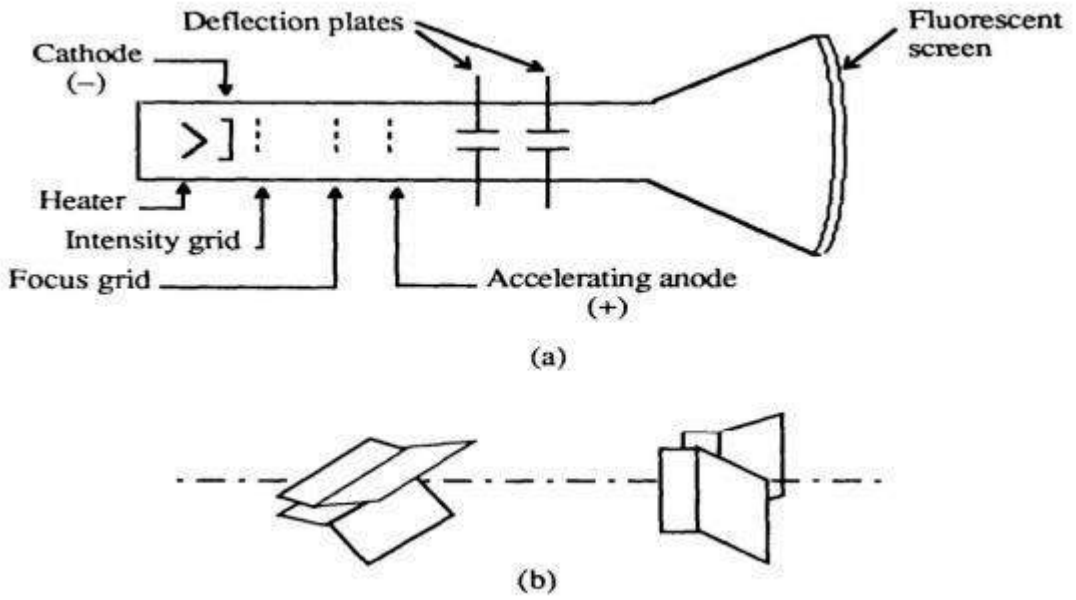



Figure 1. Cathode-ray tube: (a) schematic, (b) detail of the deflection plates.

The cathode ray is a beam of electrons which are emitted by the heated cathode (negative electrode) and accelerated toward the fluorescent screen. The assembly of the cathode, intensity grid, focus grid, and accelerating anode (positive electrode) is called an electron gun. Its purpose is to generate the electron beam and control its intensity and focus. Between the electron gun and the fluorescent screen are two pair of metal plates - one oriented to provide horizontal deflection of the beam and one pair oriented to give vertical deflection to the beam. These plates are thus referred to as the horizontal and vertical deflection plates. The combination of these two deflections allows the beam to reach any portion of the fluorescent screen. Wherever the electron beam hits the screen, the phosphor is excited and light is emitted from that point. This conversion of electron energy into light allows us to write with points or lines of light on an otherwise darkened screen. In the most common use of the oscilloscope the signal to be studied is first amplified and then applied to the vertical (deflection) plates to deflect the beam vertically and at the same time a voltage that increases linearly with time is applied to the horizontal (deflection) plates thus causing the beam to be deflected horizontally at a uniform (constant> rate. The signal applied to the vertical plates is thus displayed on the screen as a function of time. The horizontal axis serves as a uniform time scale. The linear deflection or sweep of the beam horizontally is accomplished by use of a sweep generator that is incorporated in the oscilloscope circuitry. The voltage output of such a generator is that of a saw tooth wave as shown in Fig. 2. Application of one cycle of this voltage difference, which increases linearly with time, to the horizontal plates causes the beam to be deflected linearly with time across the tube face. When the voltage suddenly falls to zero, as at points (a) (b) (c), etc. , the end of each sweep - the beam flies back to its initial position. The horizontal deflection of the beam is repeated periodically, the frequency of this periodicity is adjustable by external controls.

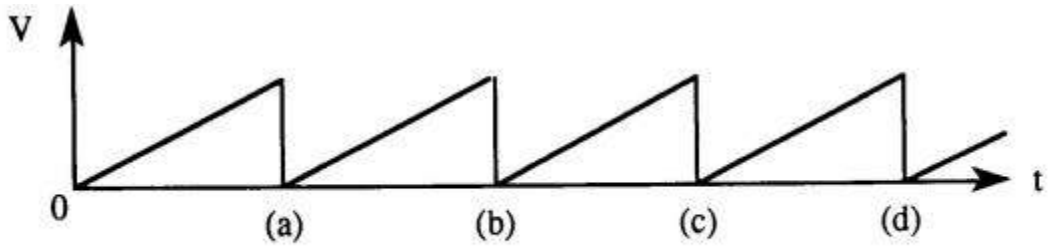



Figure. 2. Voltage difference V between horizontal plates as a function of time t.

To obtain steady traces on the tube face, an internal number of cycles of the unknown signal that is applied to the vertical plates must be associated with each cycle of the sweep generator. Thus, with such a matching of synchronization of the two deflections, the pattern on the tube face repeats itself and hence appears to remain stationary. The persistance of vision in the human eye and of the glow of the fluorescent screen aids in producing a stationary pattern. In addition, the electron beam is cut off (blanked) during fly back so that the retrace sweep is not observed. CRO Operation: A simplified block diagram of a typical oscilloscope is shown in Fig. 3. In general, the instrument is operated in the following manner. The signal to be displayed is amplified by the vertical amplifier and applied to the vertical deflection plates of the CRT. A portion of the signal in the vertical amplifier is applied to the sweep trigger as a triggering signal. The sweep trigger then generates a pulse coincident with a selected point in the cycle of the triggering signal. This pulse turns on the sweep generator, initiating the saw tooth wave form. The saw tooth wave is amplified by the horizontal amplifier and applied to the horizontal deflection plates. Usually, additional provisions signal are made for applying an external triggering signal or utilizing the 60 Hz line for triggering. Also the sweep generator may be bypassed and an external signal applied directly to the horizontal amplifier.

**CRO Controls:**

The controls available on most oscilloscopes provide a wide range of operating conditions and thus make the instrument especially versatile. Since many of these controls are common to most oscilloscopes a brief description of them follows.

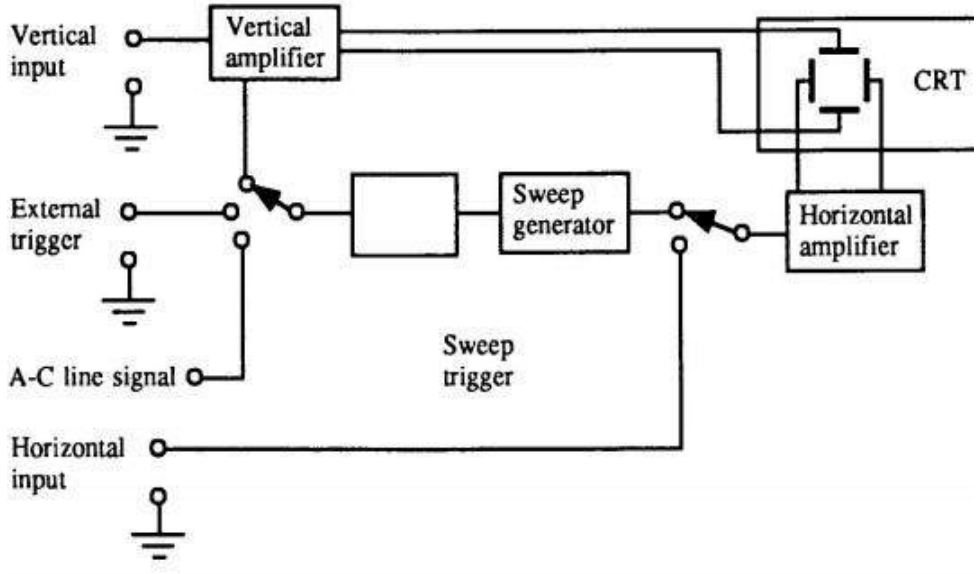



Figure 3. Block diagram of a typical oscilloscope.

**CATHODE-RAY TUBE :**

Power and Scale Illumination: Turns instrument on and controls illumination of the graticule.
Focus: Focus the spot or trace on the screen.
Intensity: Regulates the brightness of the spot or trace.

**VERTICAL AMPLIFIER SECTION**

Position: Controls vertical positioning of oscilloscope display.
Sensitivity: Selects the sensitivity of the vertical amplifier in calibrated steps.
Variable Sensitivity: Provides a continuous range of sensitivities between the calibrated steps. Normally the sensitivity is calibrated only when the variable knob is in the fully clockwise position.
AC-DC-GND: Selects desired coupling (ac or dc) for incoming signal applied to vertical amplifier, or grounds the amplifier input. Selecting dc couples the input directly to the amplifier; selecting ac send the signal through a capacitor before going to the amplifier thus blocking any constant component.

**HORIZONTAL-SWEEP SECTION :**

Sweep time/cm: Selects desired sweep rate from calibrated steps or admits external signal to horizontal amplifier.
Sweep time/cm Variable: Provides continuously variable sweep rates. Calibrated position is fully clockwise.
Position: Controls horizontal position of trace on screen.
Horizontal Variable: Controls the attenuation (reduction) of signal applied to horizontal aplifier through Ext. Horiz. Connector.
TRIGGER: The trigger selects the timing of the beginning of the horizontal sweep.
Slope: Selects whether triggering occurs on an increasing (+) or decreasing (-) portion of trigger signal.
Coupling: Selects whether triggering occurs at a specific dc or ac level. Source: Selects the source of the triggering signal.
INT - (internal) - from signal on vertical amplifier
EXT - (external) - from an external signal inserted at the EXT.
TRIG. INPUT. LINE - 60 cycle triger
Level: Selects the voltage point on the triggering signal at which sweep is triggered. It also allows automatic (auto) triggering of allows sweep to run free (free run).

**CONNECTIONS FOR THE OSCILLOSCOPE:**

Vertical Input: A pair of jacks for connecting the signal under study to the Y (or vertical) amplifier. The lower jack is grounded to the case.
Horizontal Input: A pair of jacks for connecting an external signal to the horizontal amplifier. The lower terminal is grounded to the case of the oscilloscope.
External Tigger Input: Input connector for external trigger signal.
Cal. Out: Provides amplitude calibrated square waves of 25 and 500 millivolts for use in calibrating the gain of the amplifiers. Accuracy of the vertical deflection is + 3%. Sensitivity is variable.
Horizontal sweep should be accurate to within 3%. Range of sweep is variable.
Operating Instructions:
Before plugging the oscilloscope into a wall receptacle, set the controls as follows:
(a)Power switch at off
(b)Intensity fully counter clockwise
(c)Vertical centering in the center of range
(d)Horizontal centering in the center of range
(e)Vertical at 0.2
(f)Sweep times 1

Plug line cord into a standard ac wall receptacle (nominally 118 V). Turn power on. Do not advance the Intensity Control. Allow the scope to warm up for approximately two minutes, and then turn the Intensity Control until the beam is visible on the screen.

**PROCEDURE:**

I. Set the signal generator to a frequency of 1000 cycles per second. Connect the output from the generator to the vertical input of the oscilloscope. Establish a steady trace of this input signal on the scope. Adjust (play with) all of the scope and signal generator controls until you become familiar with the function of each. The purpose for such "playing" is to allow the student to become so familiar with the oscilloscope that it becomes an aid (tool) in making measurements in other experiments and not as a formidable obstacle. Note: If the vertical gain is set too low, it may not be possible to obtain a steady trace.

II. Measurements of Voltage: Consider the circuit in Fig. 4(a). The signal generator is used to produce a 1000 hertz sine wave. The AC voltmeter and the leads to the vertical input of the oscilloscope are connected across the generator's output. By adjusting the Horizontal Sweep time/cm and trigger, a steady trace of the sine wave may be displayed on the screen. The trace represents a plot of voltage vs. time, where the vertical deflection of the trace about the line of symmetry CD is proportional to the magnitude of the voltage at any instant of time

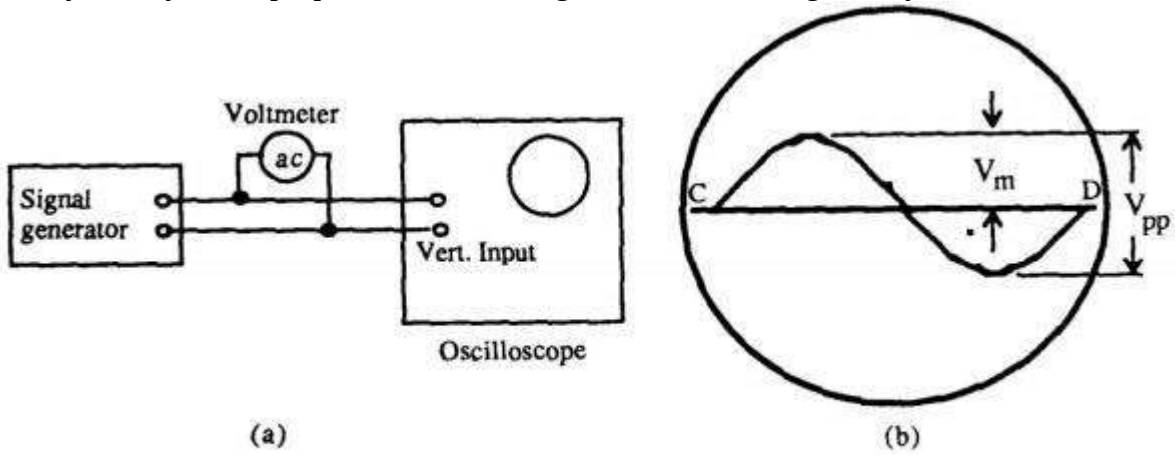



Figure 4 (a) Circuit for procedure II. (b) Trace seen on scope.

To determine the size of the voltage signal appearing at the output of terminals of the signal generator, an AC (Alternating Current) voltmeter is connected in parallel across these terminals (Fig. 4a). The AC voltmeter is designed to read the dc "effective value" of the voltage. This effective value is also known as the "Root Mean Square value" (RMS) value of the voltage. The peak or maximum voltage seen on the scope face (Fig. 4b) is Vm volts and is represented by the distance from the symmetry line CD to the maximum deflection. The relationship between the magnitude of the peak voltage displayed on the scope and the effective or RMS voltage (VRMS) read on the AC voltmeter is

$$V_{RMS} = 0.707\ Vm \text{ (for a sine or cosine wave)}$$

Thus

$$V_m = \frac{V_{RMS}}{0.707}$$

Agreement is expected between the voltage reading of the multimeter and that of the oscilloscope. For a symmetric wave (sine or cosine) the value of Vmmay be taken as 1/2 the peak to peak signal Vpp.

The variable sensitivity control a signal may be used to adjust the display to fill a convenient range of the scope face. In this position, the trace is no longer calibrated so that you cannot just read the size of the signal by counting the number of divisions and multiplying by the scale factor. However, you can figure out what the new calibration is an use it as long as the variable control remains unchanged.

Caution: The mathematical prescription given for RMS signals is valid only for sinusoidal signals. The meter will not indicate the correct voltage when used to measure non-sinusoidal signals.

III. Frequency Measurements:

When the horizontal sweep voltage is applied, voltage measurements can still be taken from the vertical deflection. Moreover, the signal is displayed as a function of time. If the time base (i.e. sweep) is calibrated, such measurements as pulse duration or signal period can be made.

Frequencies can be determined as reciprocal of the Time periods.

Set the oscillator to 1000 Hz. Display the signal on the CRO and measure the period of the oscillations. Use the horizontal distance between two points such as C to D in Fig. 4b. Set the horizontal gain so that only one complete wave form is displayed.

Then reset the horizontal until 5 waves are seen. Keep the time base control in a calibrated position. Measure the distance (and hence time) for 5 complete cycles and calculate the frequency from this measurement. Compare you result with the value determined above.

Repeat your measurements for other frequencies of 150 Hz, 5 kHz, 50 kHz as set on the signal generator

IV. Lissajous Figures:

When sine-wave signals of different frequencies are input to the horizontal and vertical amplifiers a stationary pattern is formed on the CRT when the ratio of the two frequencies is an integral fraction such as 1/2, 2/3, 4/3, 1/5, etc. These stationary patterns are known as Lissajous figures and can be used for comparison measurement of frequencies.

Use two oscillators to generate some simple Lissajous figures like those shown in Fig. 5. You will find it difficult to maintain the Lissajous figures in a fixed configuration because the two oscillators are not phase and frequency locked. Their frequencies and phase drift slowly causing the two different signals to change slightly with respect to each other.

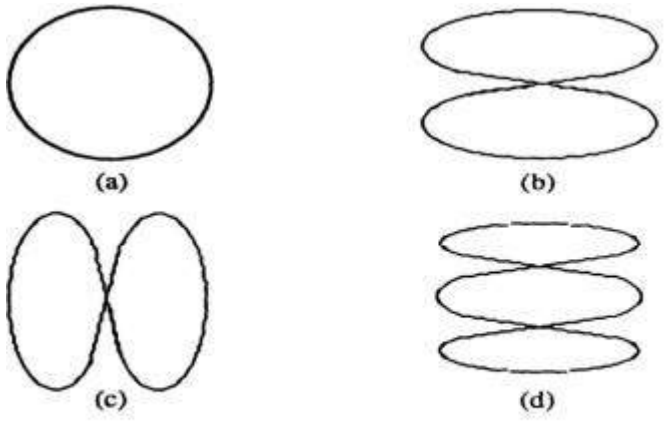



Figure 5. Lissajous figures for horizontal-to-vertical frequency ratios of: (a) 1:1, (b) 2:1, (c) 1:2, and (d) 3:1.

V. Testing what you have learned:

Your instructor will provide you with a small oscillator circuit. Examine the input to the circuit and output of the circuit using your oscilloscope. Measure such quantities as the voltage and frequencies of the signals. Specify if they are sinusoidal or of some other wave character. If square wave, measure the frequency of the wave. Also, for square waves, measure the on time (when the voltage is high) and off time (when it is low).

Result:- Study is completed

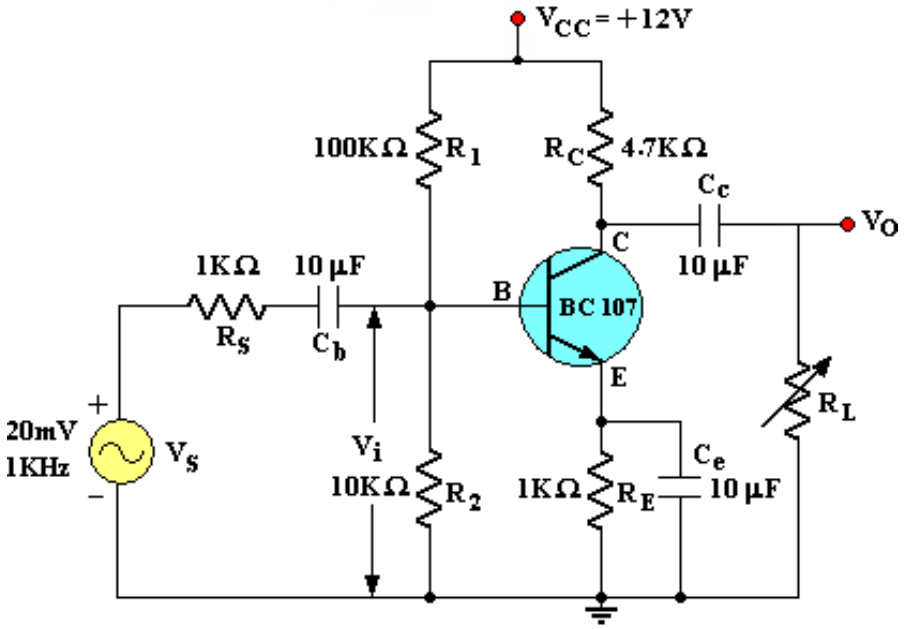
Precautions: 1.Operate cro carefully
2.Take all reading carefully
3.Use correct power supply

**VIVA Questions:**

1. Explain what is a cathode ray oscilloscope (CRO)?
A CRO is an electronic device with a CRT as its main component and other associated circuits consisting of a power supply unit, a sawtooth-wave generator, horizon and vertical amplifiers .
2. How is CRO superior to ordinary measuring instruments?
CRO is an electronic device that gives graphical representation of alternating quantities under examination. The CRO gives very accurate measurements and is free from the errors introduced by the moving parts. It is also from damping mechanisms and other inertia containing parts.
3. For Explain what vertical and horizontal plates are provide in a CRO?
Horizontal and vertical plates are provided between electron gun and screen to deflect the beam according to the input signal.
4. For what a triggering circuit is provided in a CRO?
In a CRO, a triggering circuit is provided for synchronizing two types of deflections so that horizontal deflection starts at the same point of the input vertical signal each time it sweeps.
5. Explain what are the essential components of a CRT?
The essential components of a CRT are electron gun, focusing and accelerating anodes, horizontal and vertical deflection plates, and evacuated glass envelope with phosphorescent screen.
6. For Explain what electron gun assembly is provided in CRT?
The sole function of an electron gun assembly in a CRO is to provide a narrow and sharply focused electron beam with is accelerated towards the phosphor screen.
7. Explain why is the grid in a CRO provided with a hole in it?
The hole in a grid of a CRO is provided to allow passage for electrons through it and concentrate the beam of electrons along the axis of the tube
8. Explain what is meant by the deflection sensitivity of a CRO?
The deflection sensitivity of a CRO is defined as the vertical deflection of the beam on the screen per unit deflecting voltage.
9. Explain what is meant by the deflection factor of a CRO?
The deflection factor of a CRO is the reciprocal of the deflection sensitivity.
10. Explain what is Astigmatism control?
Astigmatism control is an adjustment that will provide sharp focus over the entire screen.
11. Explain what is graticule?
Graticule is a scale on transparent material that is fitted to the face of CRT for the purpose of measurement.
12. Explain what is auadag?
Coating of a conducting material, known as aquadag, is provided over the interior surface of CRT in order to accelerate the electron beam after passing between the deflation plates and to collect electrons produced by the secondary emission when electron beam strikes the screen.
13. Explain what is meant by retrace time?
Retrace time is the time required by the electron beam to return to its original position on a CRT screen after being deflected to the right by a saw tooth waveform.
14. Explain what is sweep time?
8Sweep time is time duration during which the beam is swept from left to right on the screen of a CRT by the linearly increasing saw tooth voltage.
15. Explain what is a Lissajous pattern?
Lissajous pattern is a pattern that results from applying periodic signals to the deflection plates of a CRO.

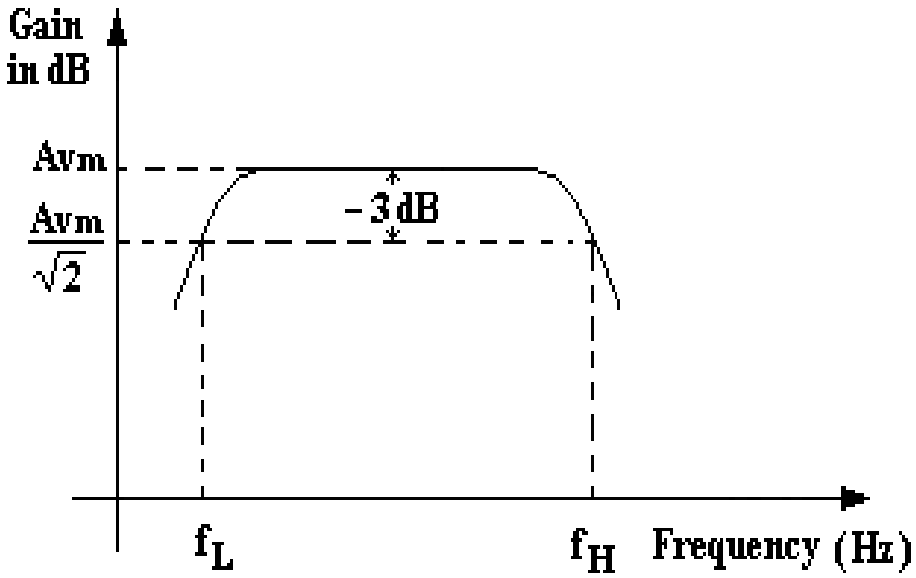
***

**CIRCUIT DIAGRAMS:**




Common Emitter Transistor Amplifier

**MODEL GRAPH:**



# 8. BJT CE AMPLIFIER

**Exp. No:…….** **Date:……**

**AIM:** To Find the frequency response of a Common Emitter Transistor Amplifier and to find the Bandwidth from the Response, Voltage gain, Input Resistance, output resistance.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | Transistor | BC107 | 1 |
| 3 | Resistors | 1KΩ | 2 |
| 4 | Resistors | 100kΩ,10KΩ, 4.7KΩ. | Each 1 |
| 5 | Capacitors | 10μf | 3 |
| 6 | Potentio Meter | -- | 1 |
| 7 | Signal Generator | ( 0 – 1MHz) | 1 |
| 8 | Dual Trace CRO | 20MHz | 1 |
| 9 | Bread Board and connecting wires | -- | 1 Set |

**THEORY:**

Bipolar junction transistor (BJT) is a 3 terminal (emitter, base, collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely emitter junction and collector junction.

In Common Emitter configuration the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between $V_{BE}$ and $I_B$ at constant $V_{CE}$ in CE configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between $V_{CE}$ and $I_C$ at constant $I_B$ in CE configuration.

**PROCEDURE:**

1. Connect the circuit as per the Fig.1.,Apply Vcc of 12 Volts DC.
2. Apply I/P Voltage of 20mV at 1KHz from the Signal Generator and observe the O/P on CRO.
3. Vary the frequency from 50 Hz to 1MHz in appropriate steps and note down the corresponding O/P Voltage Vo in a tabular form .

4. Calculate the Voltage Gain Av = Vo/Vs and note down in the tabular form.
5. Plot the frequency (f) Vs Gain (Av) on a Semi-log Graph sheet
6. Draw a horizontal line at 0.707 times Av and note down the cut off points and the Bandwidth is given by B.W = $f_2 - f_1$.

**INPUT RESISTANCE Ri:**

1. Apply I/P Voltage of 20mV at 1KHz from the Signal Generator and observe voltage Vi across R2 on CRO.
2. Without Disturbing the setup note Vi.
3. find Ii = (Vs – Vi) / Rs and Ri= Vi / Ii Ohms.

**OUTPUT RESISTANCE ($R_O$):**

1. Apply I/P Voltage of 50mV at 1KHz from the Signal Generator and observe the o/p on CRO
2. Connect a Potentio meter across the O/P terminals and without disturbing Vs adjust the potentiometer such that o/p falls to $V_0/2$
3. The Resistance of the potentiometer is equal to Ro.

**RESULT:**

| | | | |
|---|---|---|---|
| BandWidth | B.W | $= f_2 - f_1 =$ | Hz |
| Voltage Gain | Av | = | |
| Input Resistance | Ri | = | ohms |
| Output Resistance | Ro | = | ohms |

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start
3. All the contacts must be intact

**TABULAR FORMS:**

I/P Voltage, $V_s$ = 20mV

| S.No | Frequency (Hz) | O/P Voltage, Vo (V) | Voltage Gain Av =Vo/Vi | Av in dB = 20 log (Av) |
|---|---|---|---|---|
| 1 | 100 | | | |
| 2 | 200 | | | |
| 3 | 300 | | | |
| 4 | 500 | | | |
| 5 | 700 | | | |
| 6 | 1K | | | |
| 7 | 3K | | | |
| 8 | 5K | | | |
| 9 | 7K | | | |
| 10 | 10K | | | |
| 11 | 30K | | | |
| 12 | 50K | | | |
| 13 | 70K | | | |
| 14 | 100K | | | |
| 15 | 300K | | | |
| 16 | 500K | | | |
| 17 | 700K | | | |
| 18 | 1M | | | |

**VIVA QUESTIONS:**

1. What is an Amplifier?

2. How many types of an Amplifiers?

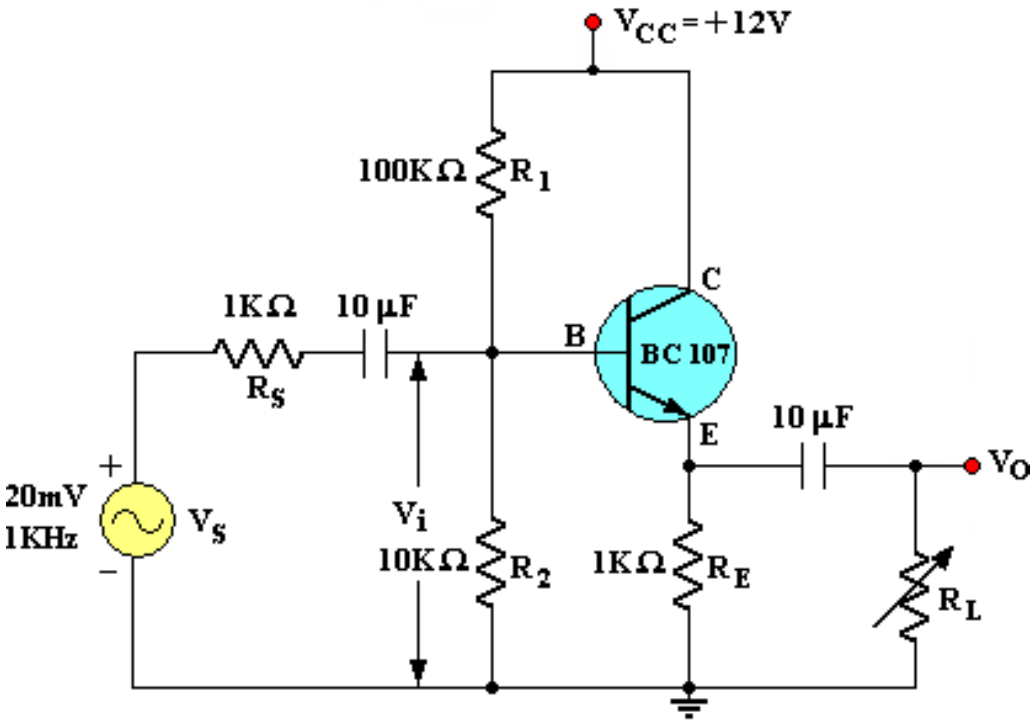
3. What is meant Band width, Lower cut-off and Upper cut-off frequency?

4. How much phase shift for CE Amplifier?

5. What are the applications?

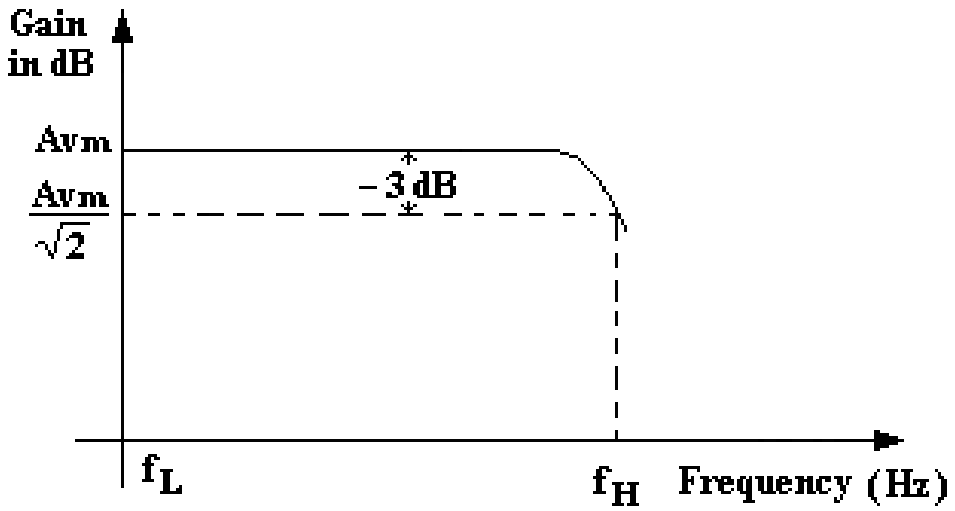
6. Draw the Equivalent circuit for low frequencies?

**CIRCUIT DIAGRAMS:**




Common Collector Transistor Amplifier

**MODEL GRAPH:**



# 9. EMITTER FOLLOWER – CC AMPLIFIER

**Exp. No:…….** **Date:……**

**AIM:** To Find the frequency response of a Common Collector Transistor Amplifier and to find the Bandwidth from the Response, Voltage gain, Input Resistance, output resistance

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Dual Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | Transistor | BC-107 | 1 |
| 3 | Capacitors | 10μf | 2 |
| 4 | Resistors | 100kΩ, 10KΩ | Each 1 |
| 5 | Resistors | 1KΩ | 2 |
| 6 | Potentio Meter | - | 1 |
| 7 | Bread Board and connecting wires | - | 1 Set |
| 8 | Signal Generator | ( 0 – 1MHz) | 1 |
| 9 | Dual Trace CRO | 20MHz | 1 |

**THEORY:**

It is called the *common-collector* configuration because (ignoring the power supply battery) both the signal source and the load share the collector lead as a common connection point.

It should be apparent that the load resistor in the common-collector amplifier circuit receives both the base and collector currents, being placed in series with the emitter. Since the emitter lead of a transistor is the one handling the most current (the sum of base and collector currents, since base and collector currents always mesh together to form the emitter current), it would be reasonable to presume that this amplifier will have a very large current gain. This presumption is indeed correct: the current gain for a common-collector amplifier is quite large, larger than any other transistor amplifier configuration.

Unlike the common-emitter amplifier from the previous section, the common-collector produces an output voltage in *direct* rather than *inverse* proportion to the rising input voltage.. As the input voltage increases, so does the output voltage. Moreover, a close examination reveals that the output voltage is nearly *identical* to the input voltage, lagging behind by about 0.7 volts.

This is the unique quality of the common-collector amplifier: an output voltage that is nearly equal to the input voltage. Examined from the perspective of output voltage *change* for a given amount of input voltage *change*, this amplifier has a voltage gain of almost exactly unity (1), or 0 dB. This holds true for transistors of any β value, and for load resistors of any resistance value.

It is simple to understand why the output voltage of a common-collector amplifier is always nearly equal to the input voltage. Referring to the diode current source transistor model in Figure below, we see that the base current must go through the base-emitter PN junction, which is equivalent to a normal rectifying diode. If this junction is forward-biased (the transistor conducting current in either its active or saturated modes), it will have a voltage drop of approximately 0.7 volts, assuming silicon construction. This 0.7 volt drop is largely irrespective of the actual magnitude of base current; thus, we can regard it as being constant

**PROCEDURE:**

1. Connect the circuit as per the Fig., Apply Vcc of 12 Volts DC.
2. Apply I/P Voltage of 50mV at 1KHz from the Signal Generator and observe the O/P on CRO.
3. Vary the frequency from 50 Hz to 1MHz in appropriate steps and note down the corresponding O/P Voltage Vo in a tabular form .
4. Calculate the Voltage Gain Av = Vo/Vs and note down in the tabular form.
5. Plot the frequency (f) Vs Gain (Av) on a semi-log Graph sheet
6. Draw a horizontal line at 0.707 times Av and note down the cut off points and the Bandwidth is given by B.W = $f_2 – f_1$.

**INPUT RESISTANCE RI:**

1. Apply I/p Voltage of 50mV at 1KHz from the Signal Generator and observe Voltage Vi across R2 on CRO
2. Without Disturbing the setup note Vi
   find Ii = (Vs – Vi) / Rs and Ri= Vi / Ii Ohms.

**OUTPUT RESISTANCE RO:**

1. Apply I/p Voltage of 50mV at 1KHz from the Signal Generator and observe the O/P on CRO

**TABULAR FORMS:**

I/P Voltage, $V_s$ = 20mV

| S.No | Frequency (Hz) | O/P Voltage, Vo (V) | Voltage Gain Av =Vo/Vi | Av in dB = 20 log (Av) |
|---|---|---|---|---|
| 1 | 100 | | | |
| 2 | 200 | | | |
| 3 | 300 | | | |
| 4 | 500 | | | |
| 5 | 700 | | | |
| 6 | 1K | | | |
| 7 | 3K | | | |
| 8 | 5K | | | |
| 9 | 7K | | | |
| 10 | 10K | | | |
| 11 | 30K | | | |
| 12 | 50K | | | |
| 13 | 70K | | | |
| 14 | 100K | | | |
| 15 | 300K | | | |
| 16 | 500K | | | |
| 17 | 700K | | | |
| 18 | 1M | | | |

2. Connect a Potentio meter across the o/p terminals and without disturbing Vs adjust the potentiometer such that o/p falls to $V_0/2$
3. The Resistance of the potentiometer is equal to Ro.

**RESULT:**

| | | |
|---|---|---|
| Band Width | B.W = f2 – f1 = | Hz |
| Voltage Gain | Av = | |
| Input Resistance | Ri = | ohms |
| Output Resistance | Ro = | ohms |

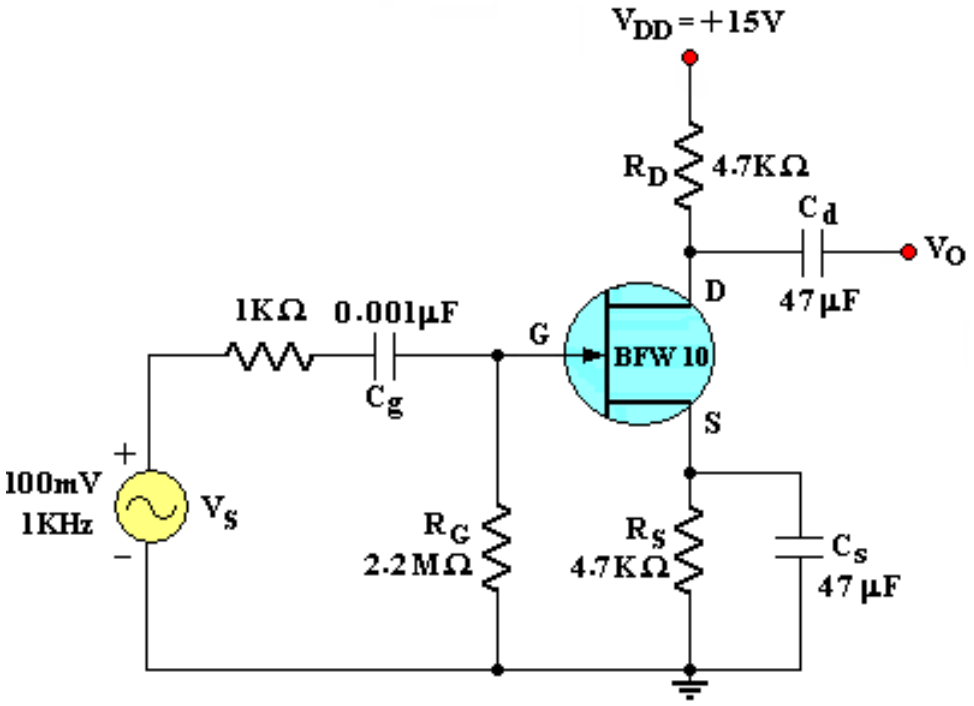
**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start
3. All the contacts must be intact

**VIVA QUESTIONS:**

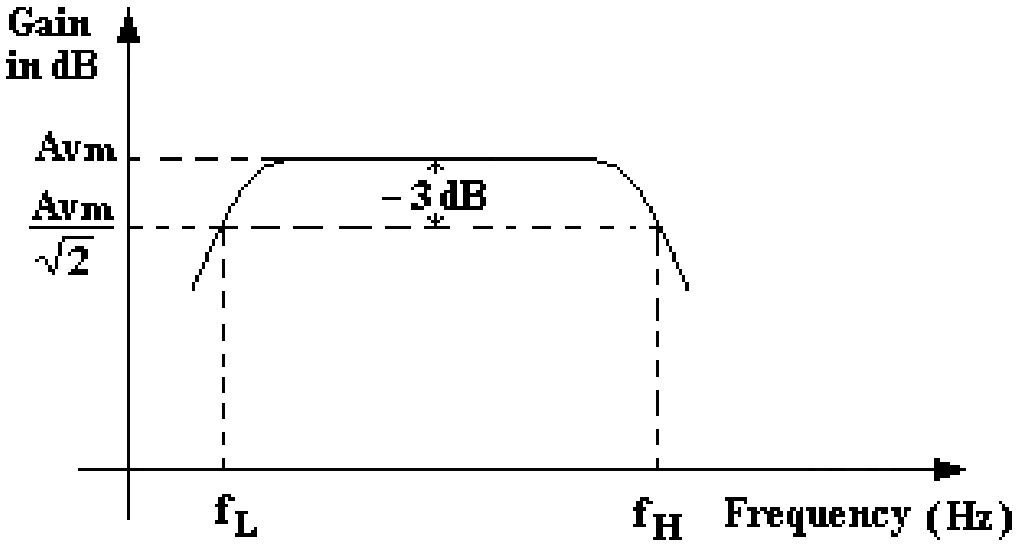
1. What is the other name for CC Amplifier?
2. What are the uses of CC Amplifier?
3. Why this amplifier has got the name Emitter Follower?
4. What is the maximum Voltage gain of an Emitter Follower?
5. Why it is used as a Buffer amplifier?

**CIRCUIT DIAGRAMS:**




Common Source JFET Amplifier

**MODEL GRAPH:**



# 10. FET-CS AMPLIFIER

**Exp. No:…….** **Date:……**

**AIM:** To study the frequency response of a Common Source Field Effect Transistor and to find the Bandwidth from the Response.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | JFET | BFW10 or 11 | 1 |
| 3 | Signal Generator | (0 – 1MHz) | 1 |
| 4 | Resistors | 1KΩ, 2.2MΩ, 4.7KΩ, 470Ω | Each 1 |
| 5 | Capacitors | 47μf | 2 |
| 6 | Capacitors | 0.001μf | 1 |
| 7 | Bread Board and connecting wires | - | 1 Set |
| 8 | Dual Trace CRO | 20MHz | 1 No |

**THEORY:**

In Common Source Amplifier Circuit Source terminal is common to both the input and output terminals. In this Circuit input is applied between Gate and Source and the output is taken from Drain and the source. JFET amplifiers provide an excellent voltage gain with the added advantage of high input impedance and other characteristics JFETs are often preferred over BJTs for certain types of applications. The CS amplifier of JFET is analogous to CE amplifier of BJT.

a common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law.

However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency

response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics. The CS–CG combination is called a cascode amplifier

**PROCEDURE:**

1. Connect the circuit as per the Fig.
2. Keep I/P Voltage at 100mV.
3. Vary the frequency from 50 Hz to 1MHz in appropriate steps and note down the corresponding source voltage Vs and o/p Voltage Vo in a tabular Form .
4. Plot the frequency (f) Vs Gain (Av) on a semi-log graph sheet and determine the Bandwidth. From the graph.

**RESULT:**

BandWidth , B.W = $f_2 - f_1$ = Hz

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start
3. All the contacts must be intact
4. For a good JFET $I_D$ will be ≥ 11.0 mA at $V_{GS}$ = 0.0 Volts if not change the JFET.

**TABULAR FORMS:**

I/P Voltage, $V_s$ = 100mV

| S.No | Frequency (Hz) | O/P Voltage, Vo (V) | Voltage Gain Av =Vo/Vi | Av in dB = 20 log (Av) |
|---|---|---|---|---|
| 1 | 50 | | | |
| 2 | 100 | | | |
| 3 | 200 | | | |
| 4 | 300 | | | |
| 5 | 500 | | | |
| 6 | 700 | | | |
| 7 | 1K | | | |
| 8 | 3K | | | |
| 9 | 5K | | | |
| 10 | 7K | | | |
| 11 | 10K | | | |
| 12 | 30K | | | |
| 13 | 50K | | | |
| 14 | 70K | | | |
| 15 | 100K | | | |
| 16 | 300K | | | |
| 17 | 500K | | | |
| 18 | 700K | | | |
| 19 | 1M | | | |

**VIVA QUESTIONS:**

1. What are the advantages of JFET over BJT?

2. Why input resistance in FET amplifier is more than BJT amplifier

3. What is a Uni-polar Device?

4. What is Pinch off Voltage?

5. What are the various FETs?

6. What is Enhancement mode and depletion mode?

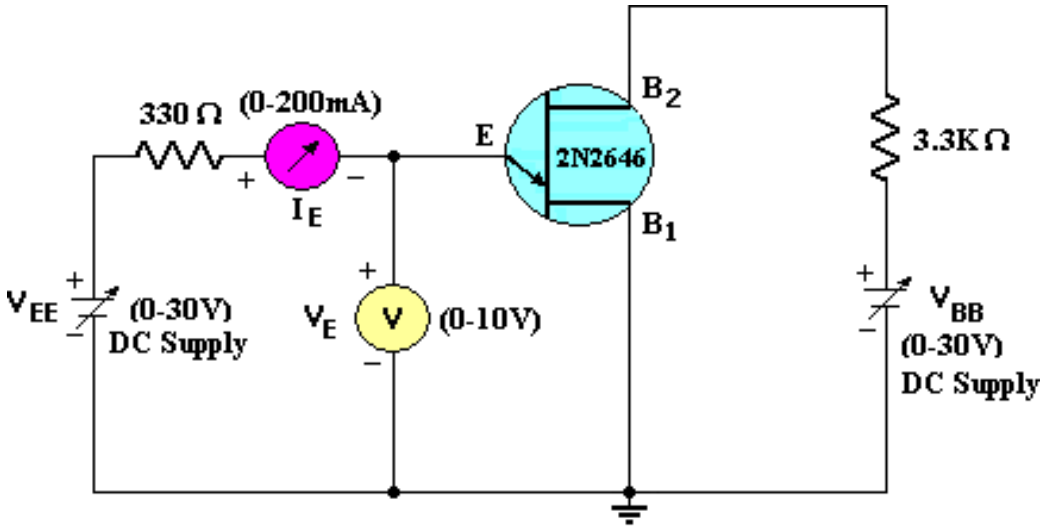
7. Draw the equivalent circuit of JFET for Low frequencies

8. Write the mathematical equation for $g_m$ in terms of $g_{mo}$.

9. Write equation of FET $I_D$ in terms of $V_{GS}$ and $V_P$.

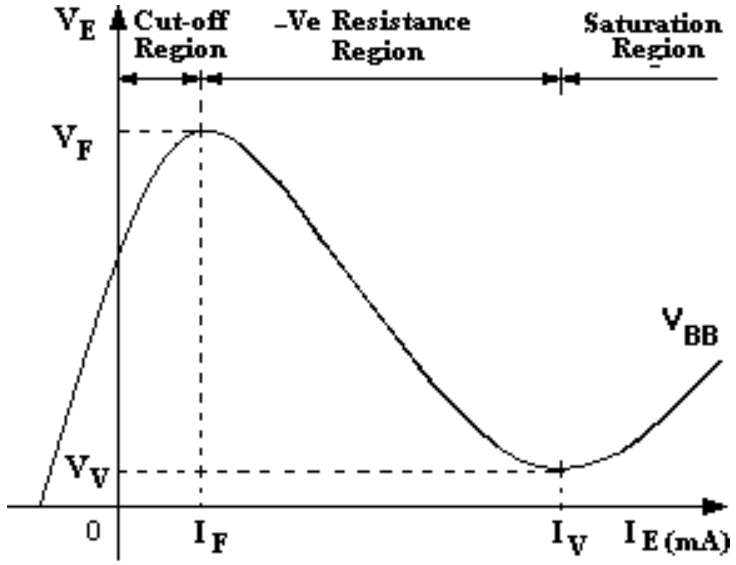
***

**CIRCUIT DIAGRAMS:**




UJT Characteristics

**MODEL GRAPHS:**




UJT Characteristics

# 11. CHARACTERISTICS OF UJT

**Exp. No:…….** **Date:……**

**AIM:** To obtain the V-I characteristics of UJT and plot its input negative resistance Characteristics also to find its Intrinsic Standoff Ratio

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Power supply | (0 – 30V) | 1 |
| 2 | Transistor | UJT 2N2646 | 1 |
| 3 | Resistors | 3.3KΩ, 330Ω | Each 1 |
| 4 | Ammeter | (0 -100mA) | 1 |
| 5 | Voltmeter | (0 – 10V) | 1 |
| 6 | Bread Board and connecting wires | - | 1 Set |

**THEORY:**

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. It has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is opencircuit is called interbase resistance. The original UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length.

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches Vp, the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point , $V_{EB}$ proportional to $I_E$.

**PROCEDURE:**

1. Connect the circuit as shown in above figure.
2. Keep $V_{BB}$ = 5V, Vary $V_{EE}$ smoothly with fine control such that $V_E$ Varies in steps of 0.5 volts from zero and note down the resulting emitter current $I_E$ for each step in the tabular form.
3. Repeat the experiment for $V_{BB}$ = 7V and for $V_{BB}$ = 10V.
4. Draw the graph between $V_E$ Vs $I_E$ by keeping $V_{BB}$ constant.

**RESULT**:

**VIVA QUESTIONS:**

1. What are the applications of UJT?

2. Why UJT is called as a Relaxation Oscillator?

3. Which type of switch is used in UJT?

4. What is Intrinsic stand off ratio?

5. Why UJT is called a negative resistance device?

**TABULAR FORM:**

| $V_{BB}$ = 5V | | $V_{BB}$ = 7V | | $V_{BB}$ = 10V | |
|---|---|---|---|---|---|
| **Vs (volts)** | **$I_E$ (mA)** | **Vs (volts)** | **$I_E$ (mA)** | **Vs (volts)** | **$I_E$ (mA)** |
| | | | | | |
| | | | | | |
| | | | | | |

6. Draw the circuit schematic for UJT?

7. What are the applications of UJT in triggering circuits?

8. Write the equation for Intrinsic stand off ratio?

9. Define valley voltage in UJT?

10. How UJT can be used for firing the silicon controlled rectifiers?

11. What are applications of UJT in Bi stable circuits?

12. What is the main application of UJT?

# 12. SCR CHARACTERISTICS

**Exp. No:…….** **Date:……**

**AIM:** 1.

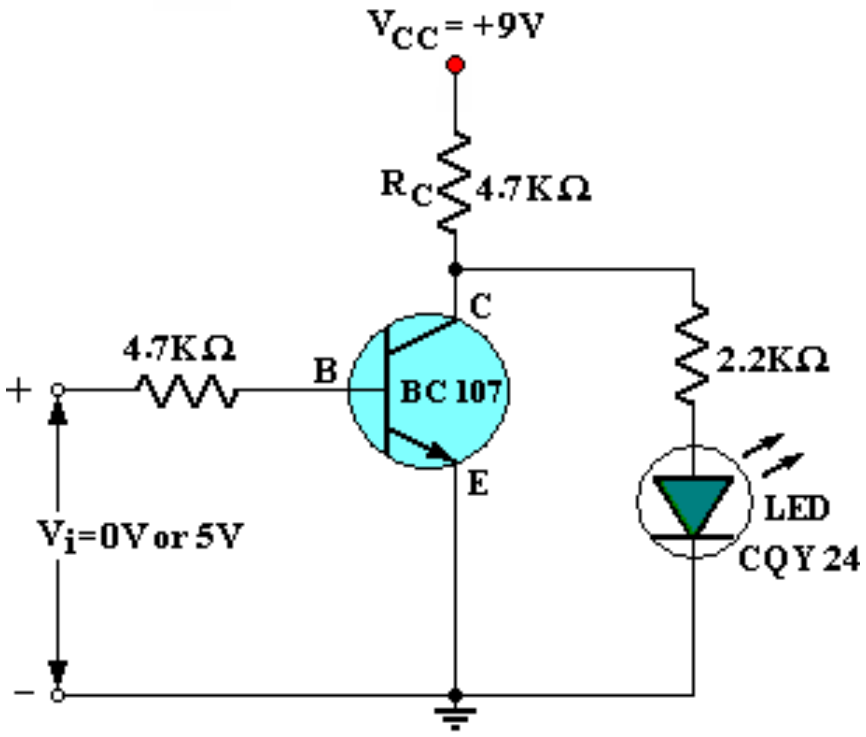
2.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |

**THEORY:**

**CIRCUIT DIAGRAM:**




Transistor as a Switch

## 13. TRANSISTOR AS A SWITCH

**Exp. No:…….** **Date:……**

**AIM:** 1. To observe the action of a Transistor as an electronic switch.

2. To measure the voltage across the transistor when it is ON and when it is OFF.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | Transistor | BC – 107 | 1 |
| 3 | Resistors | 4.7K Ω, 2.2K Ω | Each 1 |
| 4 | LED | CQY24 | 1 |
| 5 | Bread Board and connecting wires | - | 1 Set |

**THEORY:**

Transistor is used for switching operation for opening or closing of a circuit. This type solid state switching offers significant reliability and lower cost as compared with conventional relays. Both NPN and PNP transistors can be used as switches. Some of the applications use a power transistor as switching device, at that time it may necessary to use another signal level transistor to drive the high power transistor.

NPN Transistor as a Switch:

Based on the voltage applied at the base terminal of a transistor switching operation is performed. When a sufficient voltage ($V_{in} > 0.7$ V) is applied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the transistor acts as a short circuit. The collector current $V_{cc}/R_c$ flows through the transistor.

Similarly, when no voltage or zero voltage is applied at the input, transistor operates in cutoff region and acts as an open circuit. In this type of switching connection, load (here LED lamp) is connected to the switching output with a reference point. Thus, when the transistor is switched ON, current will flow from source to ground through the load.

**PROCEDURE:**

1. Construct the circuit as shown in figure.
2. Connect ‘0’ volts to the input terminals.

3. Measure the voltage across collector to emitter($V_{CE}$), collector to base($V_{CB}$) and base to emitter($V_{BE}$).
4. Connect '5' volts to the input terminals. Measure the voltage across collector to emitter($V_{CE}$), collector to base($V_{CB}$) and base to emitter($V_{BE}$).
5. Observe that the LED glows when the input terminals are supplied with '0' volts. and the LED will not glow when the input is '5' volts.

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before staring the experiment.
3. All the connections must be intact.

**RESULT:**

**TABULAR FORM:**

| Input voltage (V) | $V_{CE}$ (V) | $V_{CB}$ (V) | $V_{BE}$ (V) | Mode ON/OFF | Mode of LED |
|---|---|---|---|---|---|
| 0 V | | | | | |
| 5V | | | | | |

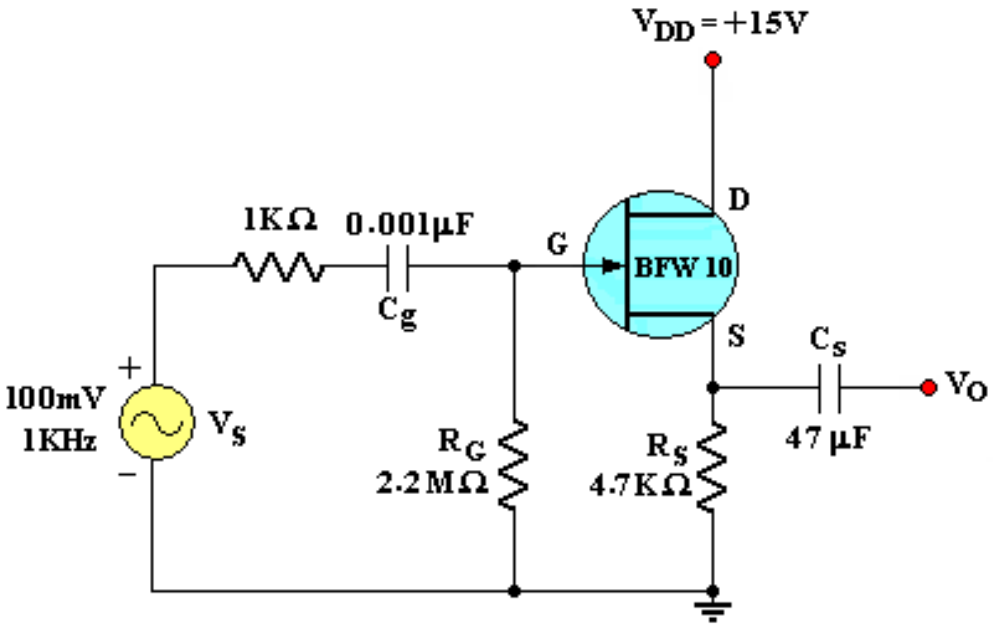
**VIVA QUESTIONS:**

1. In which region of the characteristics transistor acts as a switch?

2. What is the typical value of the collector current on ON state?

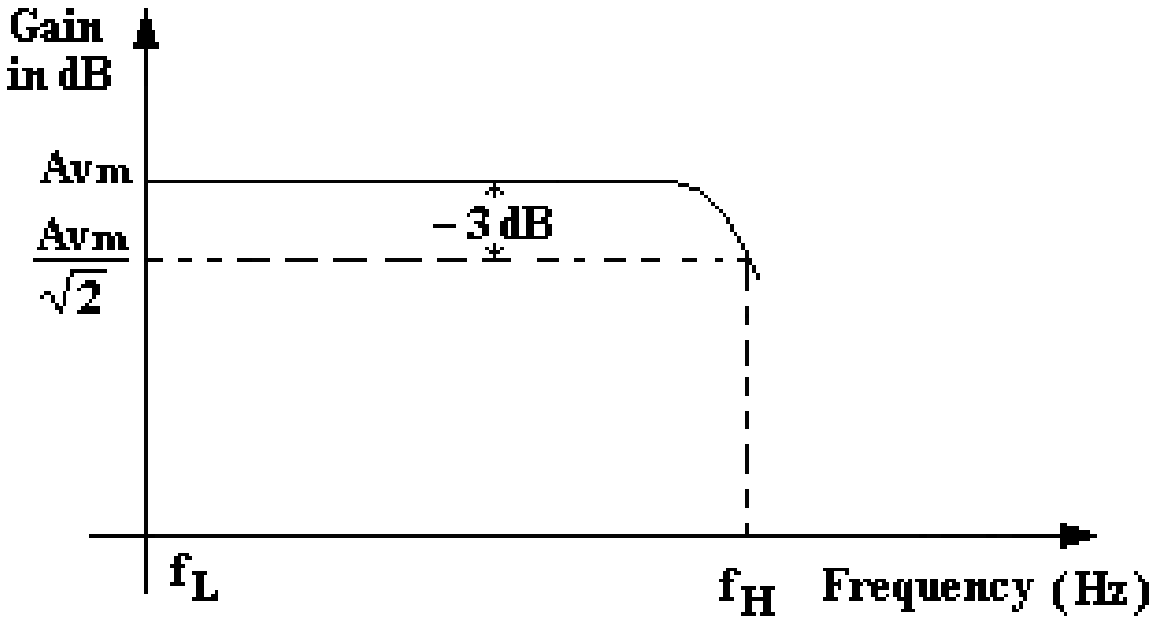
3. How the junctions of Transistor are biased in ON state and OFF state?

**CIRCUIT DIAGRAMS:**




Common Drain JFET Amplifier

**MODEL GRAPH:**



# COMMON DRAIN JFET AMPLIFIER

**Exp. No:…….** **Date:……**

**AIM:** To obtain the frequency response of a Common Drain Field Effect Transistor Amplifier and also to find its voltage gain ,Output Resistance and Bandwidth.

**APPARATUS:**

| S.No | Name | Range / Value | Quantity |
|---|---|---|---|
| 1 | Dual Regulated D.C Power supply | 0–30 Volts | 1 |
| 2 | JFET | BFW10 or 11 | 1 |
| 3 | Resistors | 2.2MΩ, 4.7KΩ | Each 2 |
| 4 | Resistors | 1KΩ | 1 |
| 5 | Capacitors | 47μf ,0.001μf | Each 1 |
| 6 | Signal Generator | ( 0 – 1MHz) | 1 |
| 7 | Bread Board and connecting wires | - | 1 Set |
| 8 | Dual Trace CRO | 20MHz | 1 No |

**THEORY:**

a **common-drain** amplifier, also known as a **source follower**, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit (NMOS) the gate terminal of the transistor serves as the input, the source is the output, and the drain is *common* to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier. This circuit is also commonly called a "stabilizer."

In addition, this circuit is used to transform impedances. For example, the Thévenin resistance of a combination of a voltage follower driven by a voltage source with high Thévenin resistance is reduced to only the output resistance of the voltage follower (a small resistance). That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a driving stage and a high load (i.e. a low resistance) presents an infinite resistance (low load) to the driving stage—an advantage in coupling a voltage signal to a large load

**PROCEDURE:**

**FREQUENCY RESPONSE:**

1. Connect the circuit as per the Fig.1. Apply $V_{DD}$ of 15 V
2. Give a signal Vs of 100 mV(P-P) at 1KHz on the I/P side and observe the O/P on CRO.

3. Vary the frequency from 50 Hz to 1MHz with proper intervals on the input side and observe the output Vo on CRO

4. Draw a graph between frequency Vs Gain on Semi-log Graph Sheet and find its Mid frequency Gain $A_{mid}$

5. Draw a horizontal line across the graph at 0.707 $A_{mid}$ and find the Bandwidth

**TO FIND $R_0$:**

1. Keep Vs = 100mV (P-P) 1KHz Signal and find Corresponding output Vo.
2. Now with out disturbing Vs Connect potentiometer across output and observe the output on CRO.
3. Adjust the value of Potentiometer Such that the output falls to the Vo/2 value.
4. Note the value of the potentiometer resistance is the Ro of the JFET CD Amplifier.

**RESULT:**

| | | | |
|---|---|---|---|
| BandWidth | B.W | $= f_2 - f_1 =$ | Hz |
| Mid band Gain | $A_{Mid}$ | = | |
| Output Resistance | Ro | = | ohms |

**PRECAUTIONS:**

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start
3. All the contacts must be intact
4. For a good JFET we will get a gain of 0.9 to 1.0 at 1KHz. If not change the JFET.

**VIVA QUESTIONS:**

1. What are the advantages of JFET over BJT?

2. Why input resistance in FET amplifier is more than BJT amplifier

3. What is a Uni-polar Device?

**TABULAR FORM:**

| S.No | Frequency (Hz) | O/P Voltage, Vo (V) | Voltage Gain Av =Vo/Vi | Av in dB = 20 log (Av) |
|---|---|---|---|---|
| 1 | 100 | | | |
| 2 | 200 | | | |
| 3 | 300 | | | |
| 4 | 500 | | | |
| 5 | 700 | | | |
| 6 | 1K | | | |
| 7 | 3K | | | |
| 8 | 5K | | | |
| 9 | 7K | | | |
| 10 | 10K | | | |
| 11 | 30K | | | |
| 12 | 50K | | | |
| 13 | 70K | | | |
| 14 | 100K | | | |
| 15 | 300K | | | |
| 16 | 500K | | | |
| 17 | 700K | | | |
| 18 | 1M | | | |

4. What is Pinch off Voltage?

5. What are the various FETs?

6. What is Enhancement mode and depletion mode?

7. Draw the equivalent circuit of JFET for Low frequencies

8. Write the mathematical equation for $g_m$ in terms of $g_{mo}$.

9. Write equation of FET $I_D$ in terms of $V_{GS}$ and $V_P$.