Switching Theory & Logic Design

LABORATORY MANUAL

R20

II / IV B.TECH (ECE)

I – SEMESTER

DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING

SIR C.R.REDDY COLLEGE OF ENGINEERING

ELURU – 534 007

Switching Theory & Logic Design

LABORATORY MANUAL

II / IV B.TECH (ECE) I – SEMESTER

LIST OF EXPERIMENTS

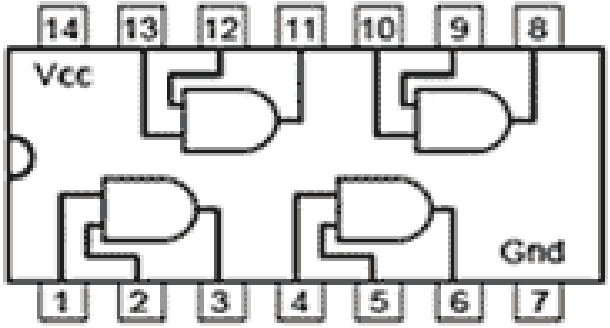
Experiments shall be carried out by using Mentor Graphics/Cadence Tools

1. Verification of truth tables of Logic gates Two input i) NOR (ii) NAND
2. Verification of truth tables of Logic gates Two input (i) OR (ii) AND (iii) Exclusive OR (iv) Exclusive NOR
3. Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer Kit
4. Verification of functional table of 3 to 8 line Decoder
5. 4 variable logic function verification using 8 to 1multiplexer
6. Design full adder circuit and verify its functional table
7. Verification of functional tables of (i) J K Edge triggered Flip –Flop (ii) D Flip –Flop
8. Design a four bit ring counter using D Flip – Flops / JK Flip Flop and verify output
9. Verify the operation of 4-bit Universal Shift Register for different Modes of operation
10. Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T-Flip-flop
11. Design MOD – 8 synchronous counter using T Flip-Flop and verify the result
12. Construct 7 Segment Display Circuit Using Decoder and 7 Segment LED and test it.

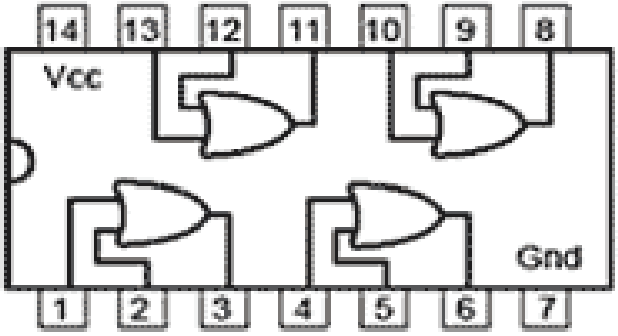
INDEX:

EXP No	NAME OF EXPERIMENT	DAY TO DAY PERFORMANCE	SIGN OF STAFF
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
TOTAL			

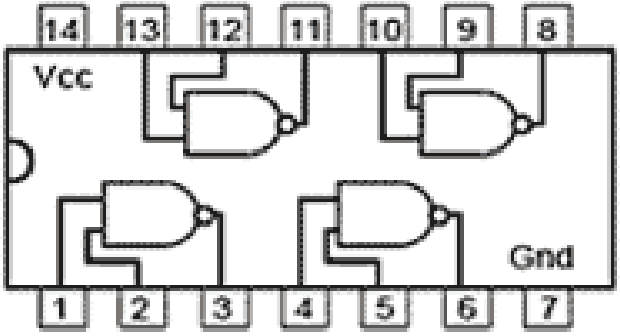
Signature of lab in charge



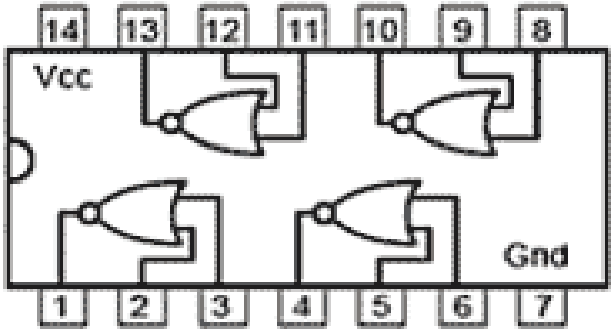
7408 Quad 2 input
AND Gates



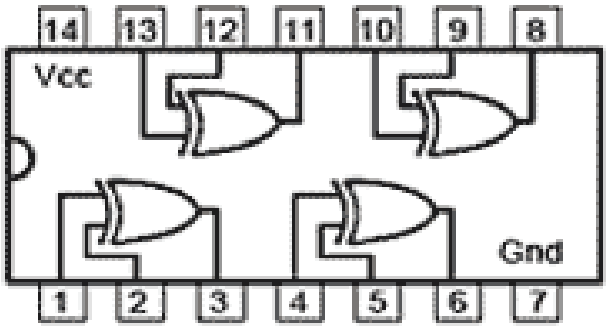
7432 Quad 2 input
OR Gates



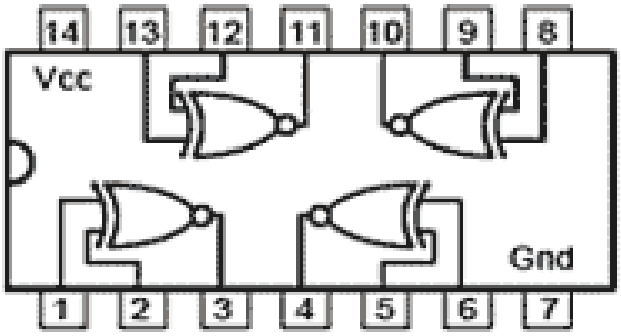
7400 Quad 2 input
NAND Gates



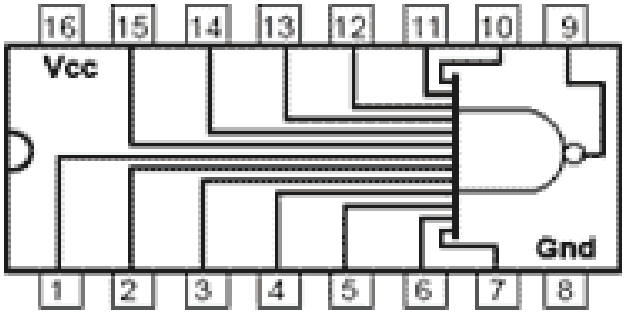
7402 Quad 2 input
NOR Gates



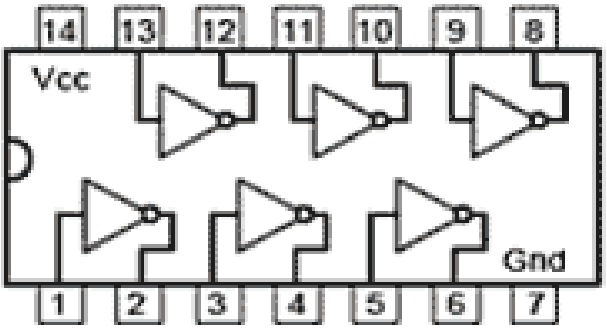
7486 Quad 2 input
XOR Gates



747266 Quad 2 input
XNOR Gates



74133 Single 13 input
NAND Gate



7404 Hex NOT Gates
(Inverters)

1. Realization of Universal gates

Aim : To Realize NAND and NOR using gates.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7408	1
3.	IC 7432	1
4	IC 7404	1

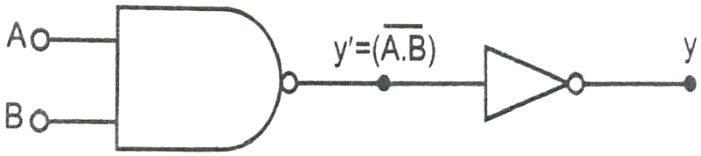
THEORY:

Procedure :

1. Derive truth table
2. Realize expression of NAND gate
3. Connect the circuit according to steps
4. Verify the truth table
5. Repeat above steps for nor
6. Derive truth table
7. Realize expression of NAND gate
8. Connect the circuit according to steps
9. Verify the truth table
10. Repeat above steps for nor

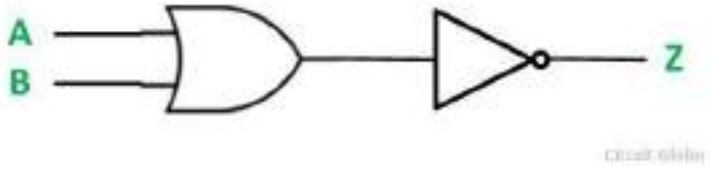
Circuit Diagram :

NAND Gate:



A	B	Y

NOR Gate:



A	B	Y

Result:

Signature of lab in charge

Exp : 2

Aim : To Realize AND,OR,NOT,EX-OR and EX-NOR gates by using only NAND and only NOR gates.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7400	2
3.	IC 7402	2

Theory:

Procedure :

Using NAND Gates

Derive truth table

Realize expression of AND gate by using number of NAND gates

Connect the circuit according to step?

Verify the truth table

Repeat above steps for OR, NOT, EX-OR and EX-NOR gates

Using NOR Gates

Derive truth table

Realize expression of AND gate by using number of NOR gates

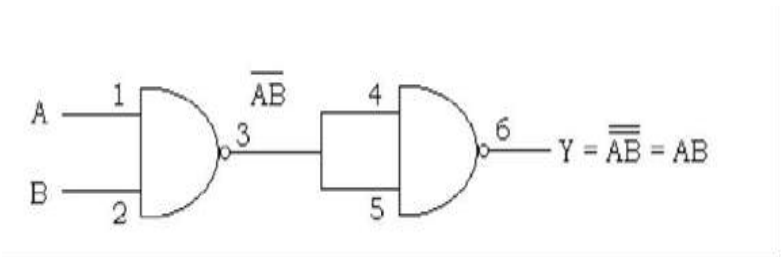
Connect the circuit according to step?

Verify the truth table

Repeat above steps for OR, NOT, EX-OR and EX-NOR gates

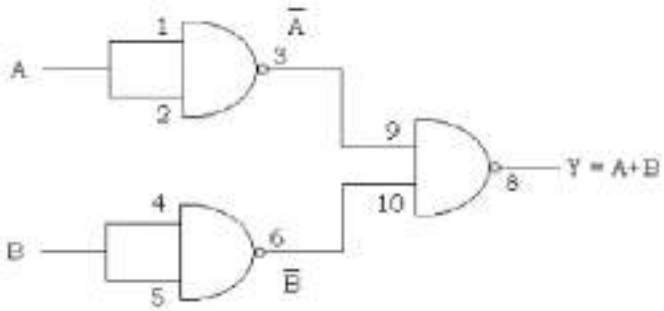
Circuit Diagram :

Realization of AND gate using only NAND gates



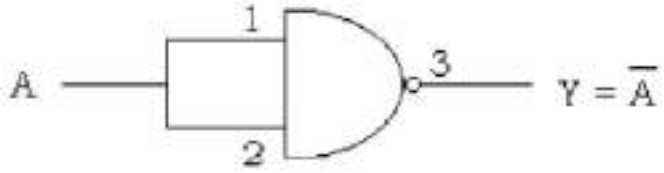
A	B	Y

Realization of OR gate using only NAND gates



A	B	Y

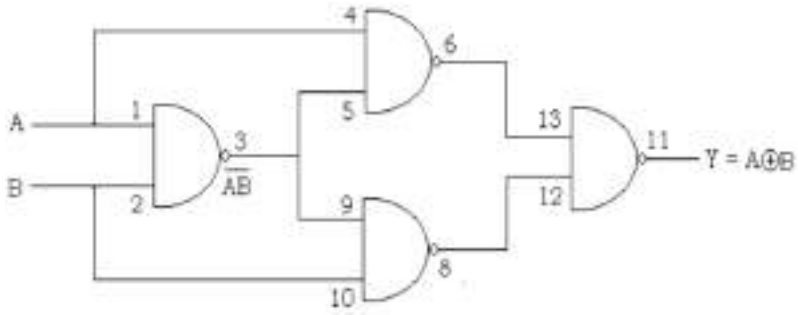
Realization of NOT gate using only NAND gates



A	**Y**

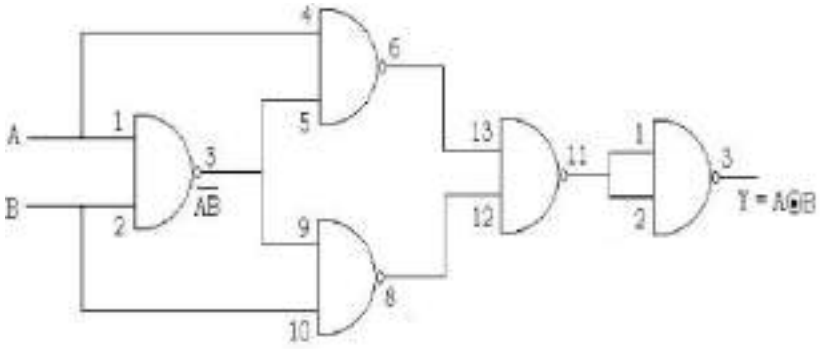
Realization of EX-OR gate using only NAND gates

A	B	Y



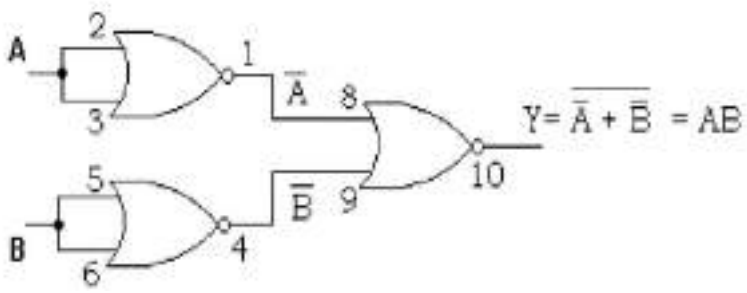
Realization of EX-NOR gate using only NAND gates

A	B	Y



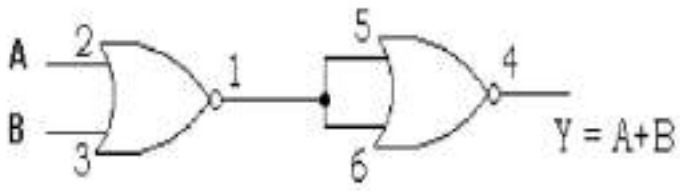
Realization of AND gate using only NOR gates

A	B	Y



Realization of OR gate using only NOR gates

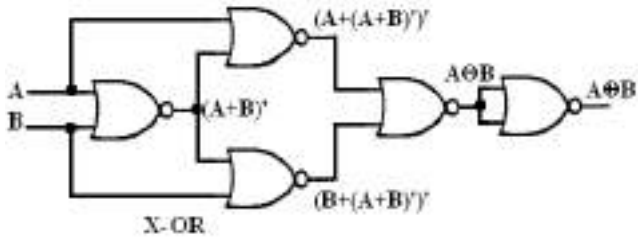
A	B	Y



Realization of NOT gate using only NOR gates

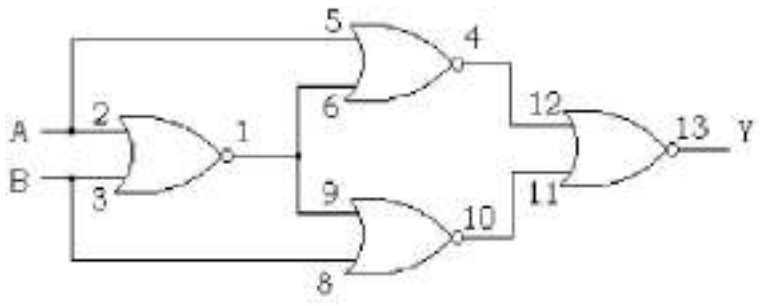
A	**Y**

Realization of EX-OR gate using only NOR gates



A	B	Y

Realization of EX-NOR gate using only NOR gates



A	B	Y

Result :

Signature of lab in charge

Exp :3

Aim : Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer Kit

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7408	1
3.	IC 7432	1
4.	IC 7486	1
5.	IC 7404	1

Theory: concepts regarding K map

Procedure :

1. First minimize the given expression.
2. Derive the truth table from the given function.
3. Realize the above simplified expression by using minimum number of gates.
4. Connect the circuit according to step 3.
5. Verify the truth table.

Problem statement:

1. F = ∑m(0,1,3,4,5,6,7,12,13,14,15) simplify

Circuit Diagram:

Result :

Signature of lab in charge

Exp :4

Aim : To implement given function by using decoders

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7442	1
3.	IC 7420	1
4.	IC 7421	1
5.	IC 7404	1

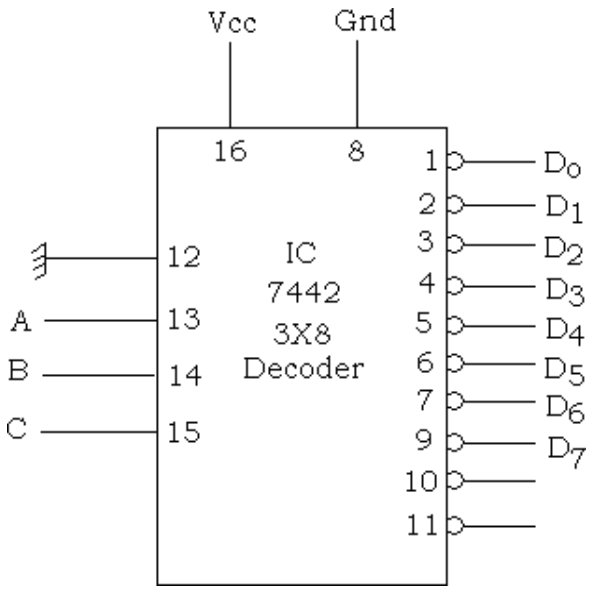
Procedure :

Using Decoders :

1. Obtain truth table from the given function
2. Realize the given function by using Decoders.
3. Connect the circuit according to step 2
4. Verify the truth table.

C	B	A	D0	D1	D2	D3	D4	D5	D6	D7
0	**0**	**0**								
0	**0**	**1**								

Circuit Diagram : **Pin Diagram of 7442 DECODER :**



Result:-

Signature of lab in charge

Exp :5

Aim : To implement given function by using Multiplexer

Apparatus and Components :

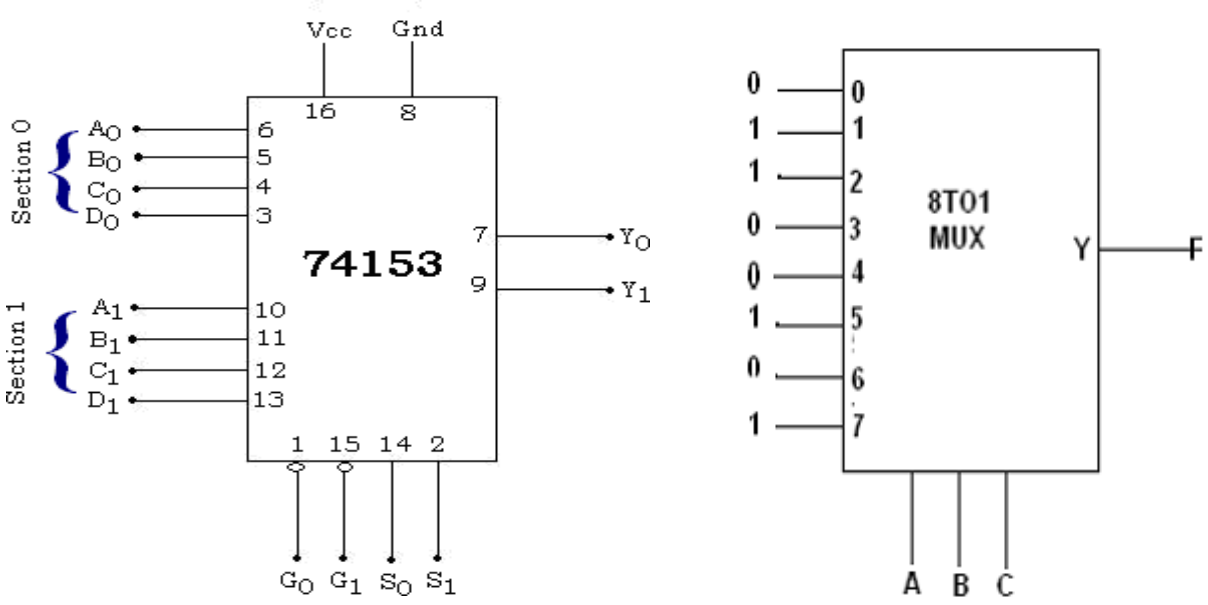
S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 74153	1
3.	IC 7420	1
4.	IC 7421	1
5.	IC 7404	1

Procedure :

Using Multiplexer :

1. Obtain truth table from the given function.
2. Obtain canonical SOP from the given function.
3. Select size of the MUX depending on the no. of input variables.
4. Derive the implementation table.
5. Realize the given function by using MUX.
6. Connect the circuit according to step 5.
7. Verify the truth table.

Circuit Diagram :Pin Diagram of 74153 MUX :



Implement the function F(A, B, C)= Σ (1, 2, 5, 7)

A	**B**	**C**	**Selected i/p**	Y (output)
0	0	0	I_0	
0	0	1	I_1	
0	1	0	I_2	
0	1	1	I_3	
1	0	0	I_4	
1	0	1	I_5	
1	1	0	I_6	
1	1	1	I_7	

Result:-

Signature of lab in charge

Exp :6

Aim : Design Full adder and verify is functional table.

Apparatus and Components :

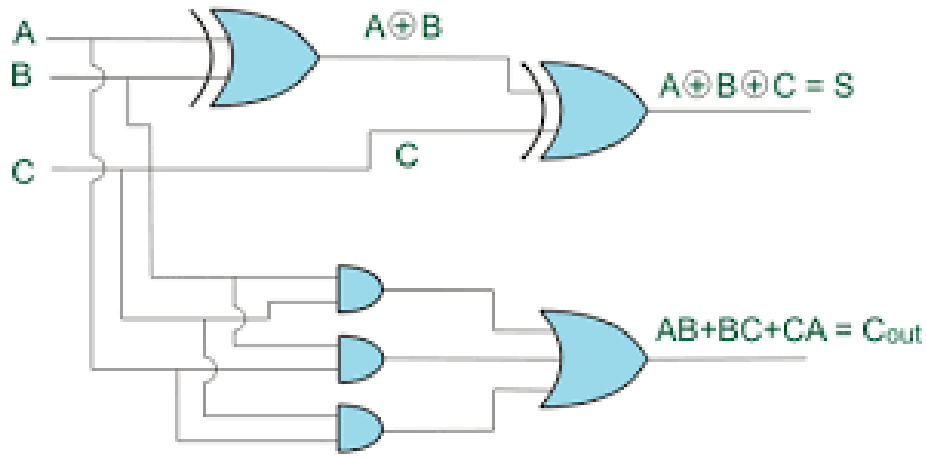
S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7408	1
3.	IC 7432	1
4.	IC 7486	1
5.	IC 7404	1

Theory: concepts regarding K map

Procedure :

1. First minimize the given expression.
2. Derive the truth table from the given function.
3. Realize the above simplified expression by using minimum number of gates.
4. Connect the circuit according to step 3.
5. Verify the truth table.

Circuit Diagram :



Truth Table:-

A	B	C	S(SUM)	Cout (carry)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Result:-

Signature of lab in charge

Exp :7

Aim: Realization of J K Flip – Flop and D K Flip – Flop

Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7476	1
3.	IC 7400	1
4.	IC 7486	1
5.	IC 7404	1

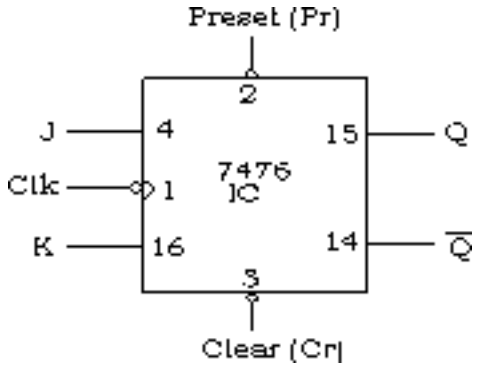
Theory :

Procedure :

1. RS flip-flop is wired as shown in fig and input signals are fed from logic input switches and the out put is monitored on the logic level out put condition indicators and the truth table is verified.
2. JK flip-flop is wired as shown in fig and the input signals are fed from logic input switches and the output is monitored on the logic level output condition indicators and the truth table is verified.
3. Verify the truth tables of D flip flop and T flip flop in the same procedure.

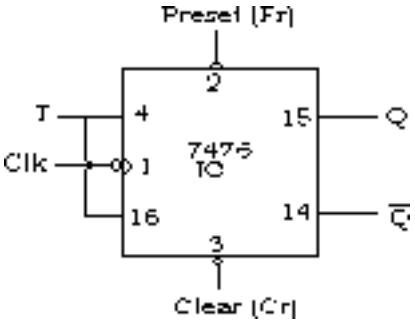
Circuit Diagram:

JK flip- flop



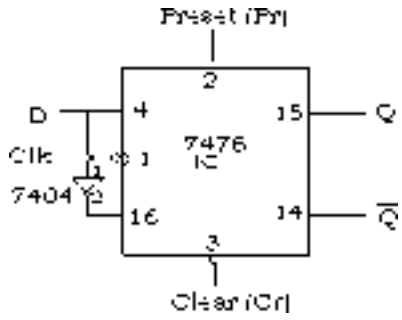
Clk	PR	CR	J	K	Theoretical	Practical
					Q_{n+1}	Q_{n+1}
0	0	1	X	X	1	
0	1	0	X	X	0	
↓	1	1	0	0	Q_n	
↓	1	1	0	1	0	
↓	1	1	1	0	1	
↓	1	1	1	1	Qn	

T flip-flop



Clk	PR	CR	T	Theoretical	Practical
				Q_{n+1}	Q_{n+1}
0	0	1	X	1	
0	1	0	X	0	
↓	1	1	0	Q_n	
↓	1	1	1	Qn	

D flip-flop



Clk	PR	CR	D	Theoretical	Practical
				Q_{n+1}	Q_{n+1}
0	0	1	X	1	
0	1	0	X	0	
↓	1	1	0	0	
↓	1	1	1	1	

Result:-

Signature of lab in charge

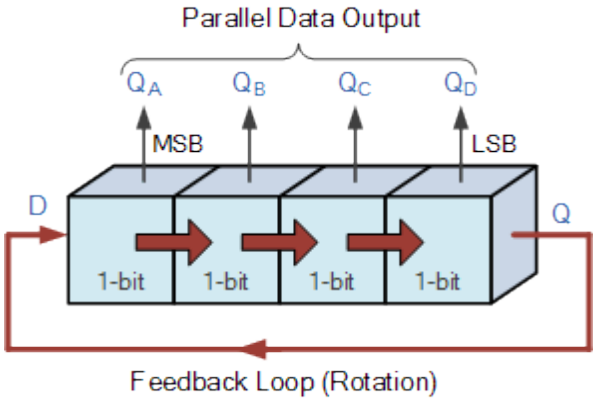
Exp :8

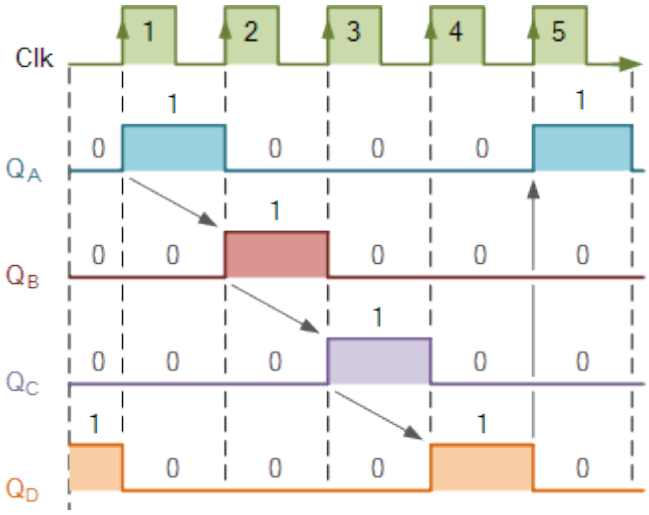
Aim :Design a four bit ring counter using D Flip-Flops /JK Flip-Flops and verify output

S.No	Name	Quantity
1.	Digital trainer	1
2	IC 7476	2
3..	IC 7404	1

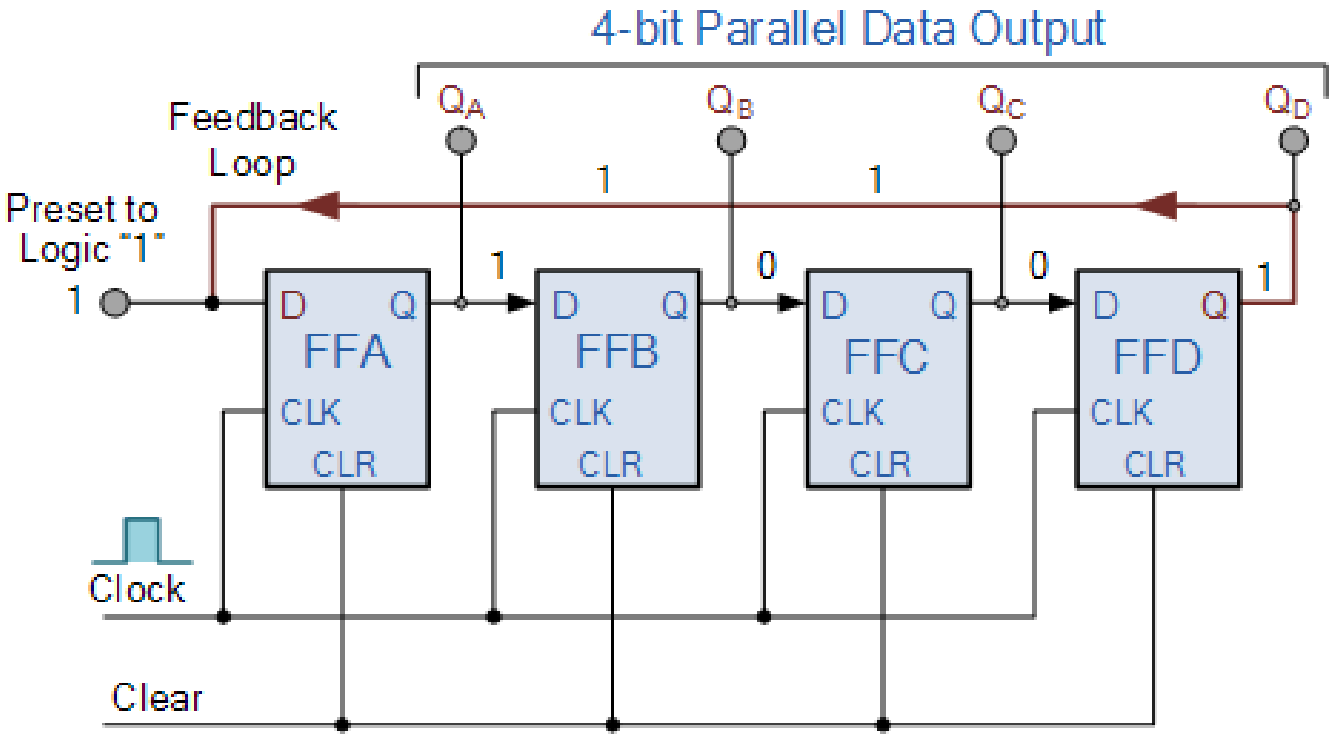
Procedure :

1. Ring counter circuit is connected as shown in the circuit diagram.
2. 1Hz clock pulse is applied to the pin shown.
3. The outputs $Q_oQ_1Q_2Q_3$ are observed and verify the truth table.





Circuit Diagram:-



Clear	Clock	QA	QB	QC	QD
1	X	0	0	0	0
0	1	**1**	0	0	0

0	1	0	1	0	0
0	1	0	0	1	0
0	1	0	0	0	1
0	1	1	0	0	0
0	1	0	1	0	0
0	1	0	0	1	0
0	1	0	0	0	1

Result:-

Signature of lab in charge

Exp :9

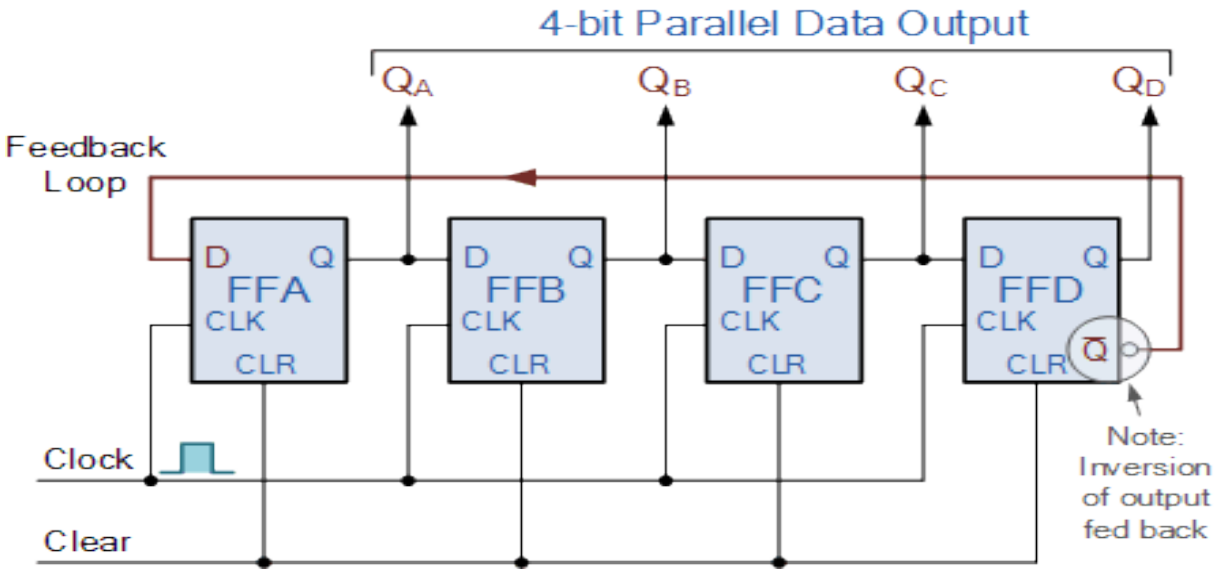
Aim: Design a four bit ring counter using D Flip-Flops /JK Flip-Flops and verify output

S.No	Name	Quantity
1.	Digital trainer	1
2	IC 7476	2
3..	IC 7404	1

Procedure :

1. Johnson Ring counter circuit is connected as shown in the circuit diagram.
2. 1Hz clock pulse is applied to the pin shown.
3. The outputs $Q_oQ_1Q_2Q_3$ are observed and verify the truth table.

Circuit Diagram:- 4-bit Johnson Ring Counter



Clear	Clock	QA	QB	QC	QD
1	X	0	0	0	0

0	1	1	0	0	0
0	1	1	1	0	0
0	1	1	1	1	0
0	1	1	1	1	1
0	1	0	1	1	1
0	1	0	0	1	1
0	1	0	0	0	1
0	1	0	0	0	0

Result:-

Signature of lab in charge

EXP:10

Aim: Verify the operation of 4-bit Universal Shift Register for different Modes of operation.

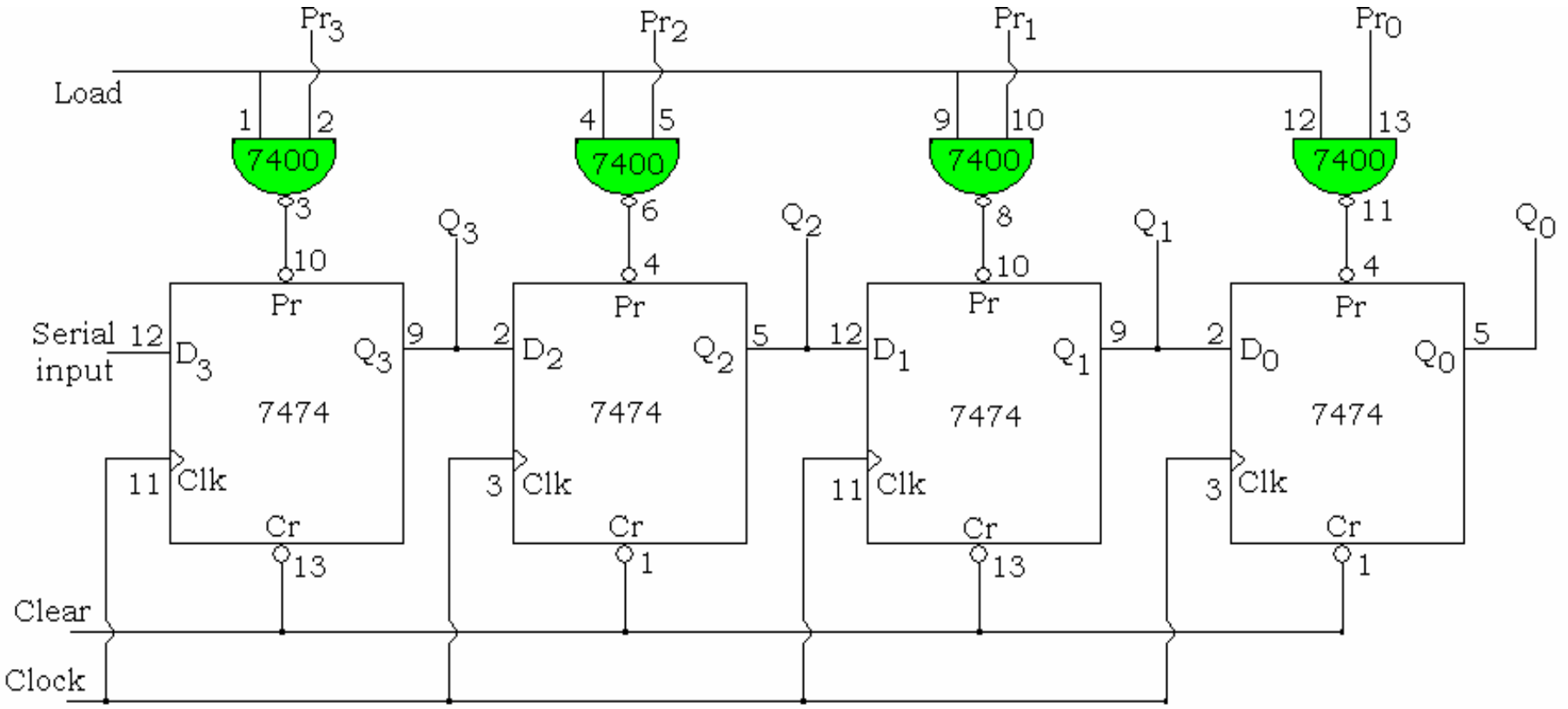
Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2	IC 7474	2
3..	IC 7400	1

Procedure :

1. Connect the circuit as shown in fig.
2. For serial loading keep load low.
3. First clear all the flip-flops by supplying clear = low

4. First enter serial input one by one, through clock pulse; we will get parallel output at $Q_3Q_2Q_1Q_o$. After applying 4 clock pulses we will get serial output.
5. For parallel input keep load = high
6. Directly apply parallel input to $P_{r3},P_{r2},P_{r1},P_{r0}$; we will get parallel output at $Q_3Q_2Q_1Q_o$. After applying 4 clock pulses we will get serial output.



4-bit Shift Register

IC 7400 Vcc = 14 Gnd = 7

IC 7474 Vcc = 14 Gnd = 7

4 – bit Shift Register Truth Table :

Serial Input Serial Output: The input is 1010.

Load	Clk	Clear	Serial i/p	Serial output Qo
0	X	0	X	0
0	1	1	0	0
0	2	1	1	0
0	3	1	0	0
0	4	1	1	**0**
0	5	1	0	**1**
0	6	1	0	**0**
0	7	1	0	**1**

Serial Input Parallel Output : The input is 1010.

Load	Clk	Clear	Serial i/p	Parallel output			
				Q3	Q2	Q1	Q0
0	X	0	X	0	0	0	0
0	1	1	0	0	0	0	0
0	2	1	1	0	0	0	0
0	3	1	0	1	0	0	0
0	4	1	1	0	1	0	0
0	5	1	0	1	0	1	0
0	6	1	0	0	1	0	1
0	7	1	0	0	0	1	0
0	8	1	0	0	0	0	1

4 – bit Shift Register Truth Table

Parallel input Serial Output : The input is 1010.

Load	Clk	Clear	Parallel i/p				Serial output Qo
			Pr3	Pr2	Pr1	Pr0	
0	X	0	X	X	X	X	0
1	X	1	1	0	1	0	0
0	1	1	X	X	X	X	1
0	2	1	X	X	X	X	0
0	3	1	X	X	X	X	1

Parallel input Parallel Output : The input is 1010.

Load	Clk	Clear	Parallel i/p				Parallel output			
			Pr3	Pr2	Pr1	Pr0	Q3	Q2	Q1	Q0
0	X	0	X	X	X	X	0	0	0	0
1	X	1	1	0	1	0	**1**	**0**	**1**	**0**
0	1	1	X	X	X	X	0	**1**	**0**	**1**
0	2	1	X	X	X	X	0	0	**1**	**0**
0	3	1	X	X	X	X	0	0	0	**1**

Result:-

Signature of lab in charge

EXP:11

Aim:- Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T-FlipFlops

Apparatus and Components :

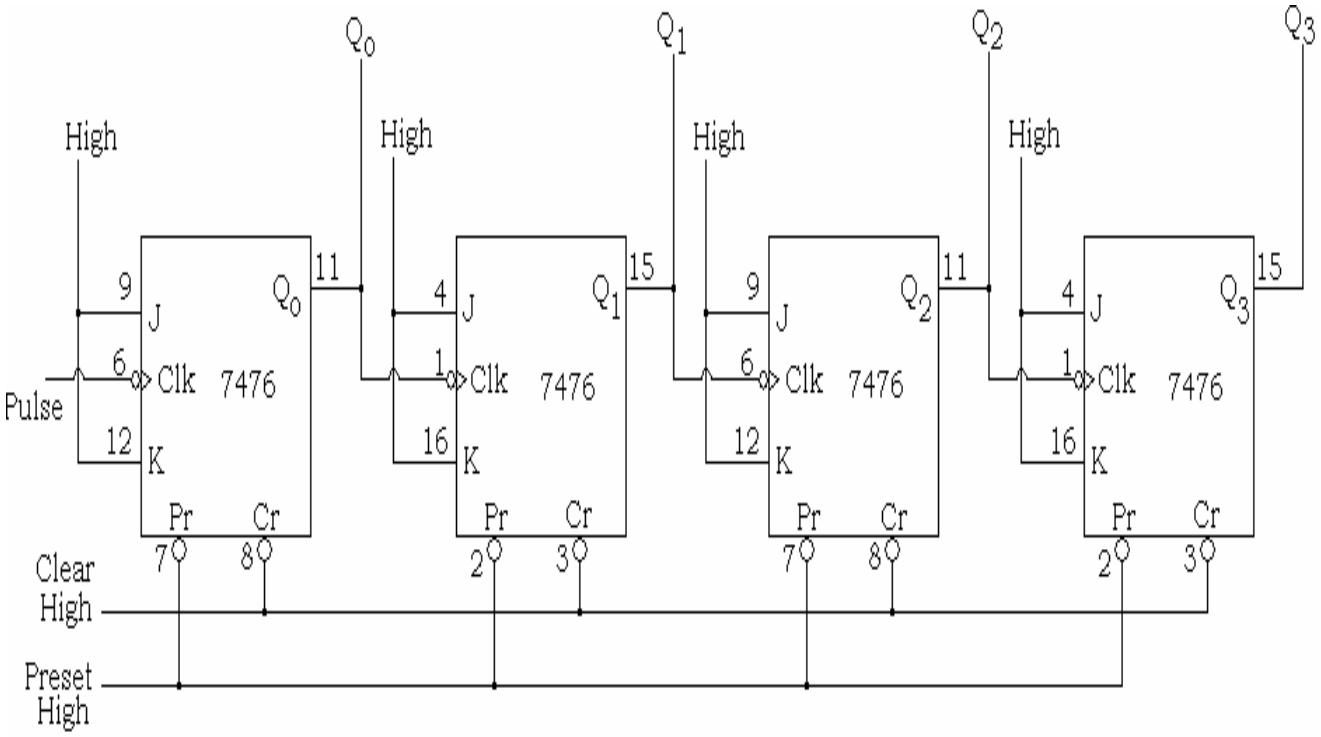
S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7476	2

Theory:

Procedure :

1. Ripple counter circuit is connected as shown in the circuit diagram.
2. 1Hz clock pulse is applied to the pin shown.
3. The outputs $Q_oQ_1Q_2Q_3$ are observed and verify the truth table.

4 – bit Ripple Counter **(VCC =5 GND=13)**



Clock pulses	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

Result:-

Signature of lab in charge

Exp:12

Aim:- Design MOD – 8 synchronous counter using T Flip-Flop and verify the result and Sketch the output waveforms.

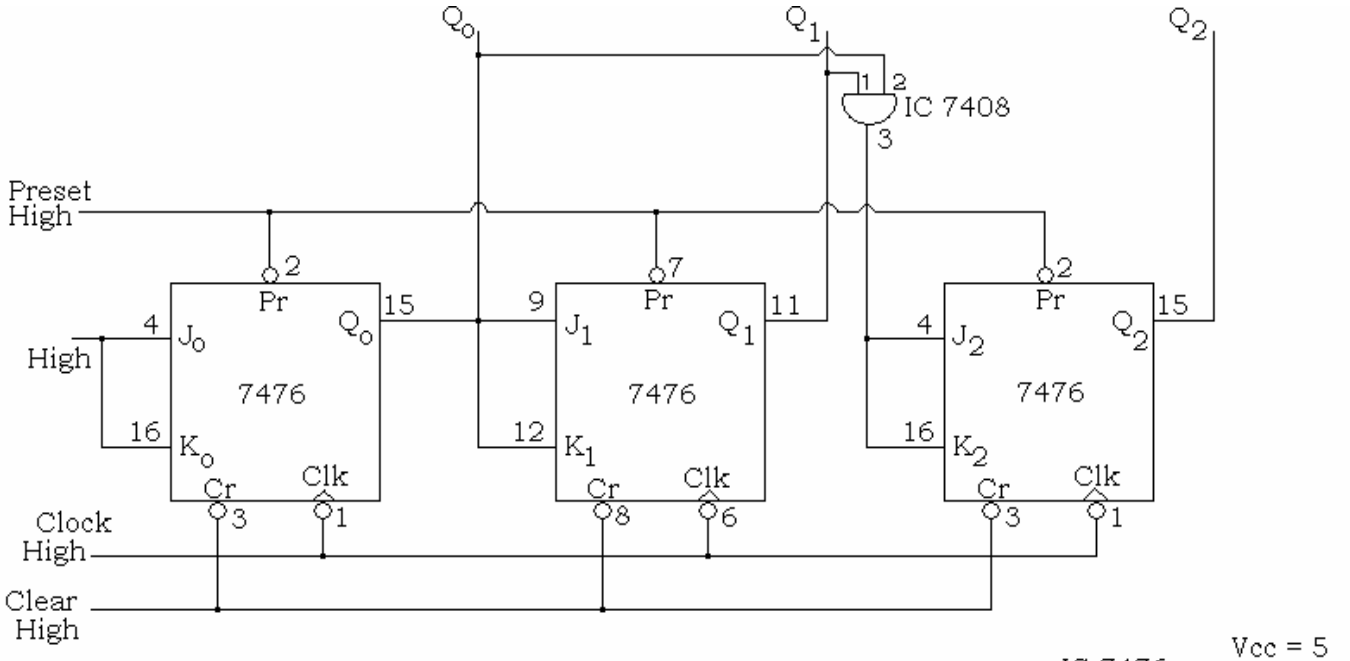
Apparatus and Components :

S.No	Name	Quantity
1.	Digital trainer	1
2.	IC 7476	2
3.	IC 7408	1

Theory

Procedure :

1. Mod- 8 Synchronous counter circuit is connected as shown in the circuit diagram.
2. 1Hz clock pulse is applied to the pin shown.
3. The outputs $Q_oQ_1Q_2Q_3$ are observed and verify the truth table.



Mod - 8 Synchronous Counter

Circuit Diagram :

Clock pulses	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Result:-

Signature of lab in charge

EXP 13

Aim :- Construct 7 Segment Display Circuit Using Decoder and 7 Segment LED and test it.

Apparatus and Components :

S.No	Name	Quantity
1.	Digital Trainer	1
2.	IC 7447	1
3.	IC FND 507	1

Theory:

Procedure :

1. Set up the Ckt as shown in fig.
2. Apply logic '0' level to LT and observe the seven segments of the LED. All the segments must be ON.
3. Apply logic '0' level to BI/RBO and observe the seven segments of the LED. All the segments must be OFF.
4. Apply logic '1' to LT and RBI and observe the number displayed on the LED for all the inputs 0000 through 1111. This is the normal decoding mode.
5. Apply logic '1' to LT and logic '0' to RBI, and observe the BI/RBO output and the number displayed on the LED for all the inputs 0000 through 1111. This is the normal decoding mode with zero blanking.

The functions of LT, RBI, RBO and BI are given below.

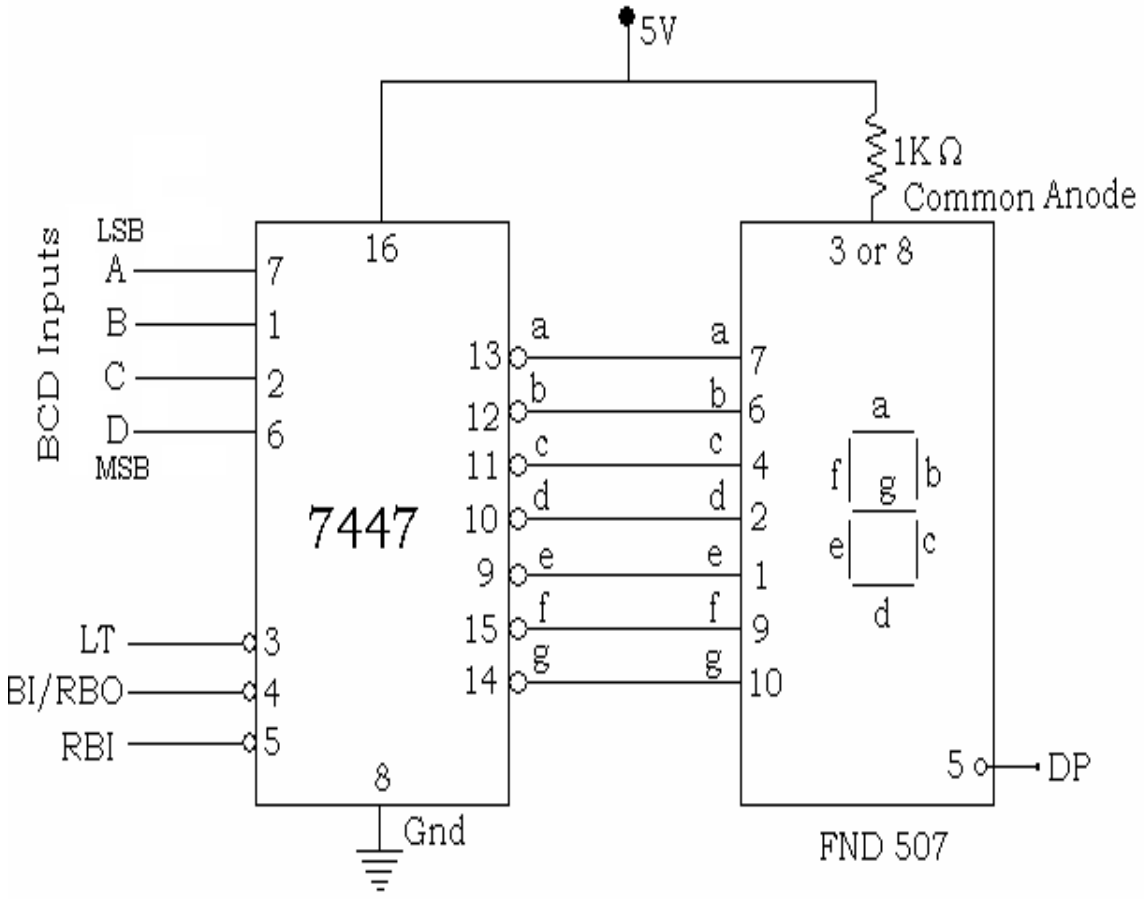
LT This is called the LAMP TEST terminal and is used for segment testing. If it is connected to logic '0' level, all the segements of the display connected to the decoder will be ON. For normal decoding operation, this terminal is to be connected to logic '1' level.

RBI For normal decoding operation, this is connected to logic '1' level. If it is connected to logic '0', the segment outputs will generate the data for normal 7-segment decoding, for all BCD inputs except Zero. Whenever the BCD inputs correspond to Zero, the 7-segment display switches off. This is used for zero blanking in multi-digit displays.

BI If it is connected to logic '0' level, the display is switched-off irrespective of the BCD inputs. This is used for conserving the power in multiplexed displays.

RBO This output is used for cascading purposes and is connected to the RBI terminal of the succeeding stage.

Circuit Diagram :



Truth Table :

D	C	B	A	a	b	c	d	e	f	g	Display Number
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	1	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	

Result :

Signature of lab in charge