Code No: R1631043

(**R16**)

(SET - 1)

III B. Tech I Semester Regular/Supplementary Examinations, March - 2021
DIGITAL IC APPLICATIONS
(Common to Electronics and Communication Engineering, Electronics and Instrumentation
Engineering, Electronics and Computer Engineering)

Time: 3 hours   Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**
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PART –A   (14 Marks)

1. a) What is CMOS logic and explain its importance?   [2M]
    b) Discuss the binding between library and components.   [2M]
    c) What is Process statement and explain its importance in Behavioral Modeling?   [2M]
    d) Write a VHDL program for half adder.   [3M]
    e) Explain the procedure to convert a T flip-flop into D flip-flop.   [3M]
    f) What is State diagram and explain its importance.   [2M]

PART –B   (56 Marks)

2. a) Draw and explain the principle of a Emitter-Coupled Logic (ECL/CML) through   [7M]
        basic ECL inverter/buffer circuit with input HIGH and LOW.
    b) Compare the characteristics of the different types of MOS inverters in terms of noise   [7M]
        margin and power dissipation.

3. a) Explain the VHDL program file structure with the syntax of a VHDL entity   [7M]
        declaration and architecture definition.
    b) Write the syntax of a VHDL component declaration and by making use of   [7M]
        component declaration write a VHDL program for a prime-number detector.

4. a) Explain the following terms in Behavioral Modeling: [6M]
        (i) Case statement,   (ii) null statement,   (iii) loop statement.
    b) Explain the concept of Inertial Delay Model along with one example.   [8M]

5. a) Design a full subtractor with logic gates and write VHDL data flow program for the   [7M]
        implementation of the above subtractor.
    b) Write VHDL code for 4-bit look ahead carry generator along with circuit diagram.   [7M]

6. a) Design an 8-bit serial-in and parallel-out shift register with flip-flops. Explain the   [7M]
        operation with the help of timing waveforms.
    b) Design a conversion circuit to convert a RS flip-flop to J-K flip-flop. Write data-flow   [7M]
        style VHDL program.

7. a) Explain the following terms in detail: (i) State Reduction, (ii) State Assignment.   [6M]
    b) Draw the block diagram of vending machine controller and write a VHDL code for it.   [8M]

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PART –A　　　　　　　　　　　　　　　　　　　(14 Marks)

1. a) List out few comparisons of BJT and CMOS Logic. [2M]

   b) Explain the program structure of VHDL Modeling. [2M]

   c) Differentiate between VHDL and Verilog HDL. [2M]

   d) List the applications of multiplexers and demultiplexers. [3M]

   e) List out few comparisons of Latches and flip flops in detail. [2M]

   f) Distinguish between Mealy and Moore machines with suitable diagrams. [3M]

PART –B　　　　　　　　　　　　　　　　　　　(56 Marks)

2. a) What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw the interface circuit and explain the operation. [7M]

   b) Derive and discuss about CMOS dynamic electrical behavior with characteristics. [7M]

3. a) Explain the differences in VHDL program structure with any other language with the help of an example. [7M]

   b) What is the importance of time dimension in VHDL? Explain its function. [7M]

4. a) Explain the following terms detail: i) Transport Delay Model,   ii) Logic Synthesis. [7M]

   b) Explain the concept of assertion statement in Behavioral Modeling along with one example. [7M]

5. a) Draw the logic symbol, arithmetic conditions, logic diagram of a commercially available MSI 74x682 8-bit comparator and model the same using VHDL program. [7M]

   b) Design a 10 to 4 encoder with inputs 1- out of 10 and outputs in BCD. Provide the data flow style VHDL program. [7M]

6. a) Draw the circuit diagram of Universal Shift Registers along with wave forms and write a VHDL code for it. [7M]

   b) Design a Johnson Counter and write a VHDL code for it along with output wave forms. [7M]

7. a) Draw the circuit diagram of FSM for serial adder and explain its operation along with VHDL code for it. [7M]

   b) Explain the following terms in detail:
   i) One hot encoding,   ii) state assignment and state table. [7M]

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SET - 3

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PART –A   (14 Marks)

1. a) What are different data types available in VHDL?   [2M]
    b) Why D flip-flop is preferred in all the sequential circuit design?   [2M]
    c) Explain about data objects in VHDL.   [2M]
    d) Explain the operation of half-adder.   [3M]
    e) What is a Johnson counter?   [3M]
    f) Compare latch and flip-flop.   [2M]

PART –B   (56 Marks)

2. a) Draw and explain the principle of an Emitter-Coupled Logic (ECL/CML) through [7M]
       basic ECL inverter/buffer circuit with input HIGH and LOW.
    b) Explain about Various TTL Families.   [7M]

3. a) Describe the modeling of 2 to 4 decoder using behavioral style of modeling. [7M]
    b) Explain various types of operators used in VHDL.   [7M]

4. a) Write a VHDL program for Full Adder using two Half Adders.   [7M]
    b) Explain the different types of delays in VHDL and explain them.   [7M]

5. a) Write a VHDL script to convert the fixed point to floating point conversion. [7M]
    b) Explain the operation of a ripple carry adder.   [7M]

6. a) Explain the operation of SR Flip-Flop.   [7M]
    b) Write the VHDL Structural program for D Latch.   [7M]

7. a) Explain the operation of Mealy machine with a neat diagram.   [7M]
    b) With an example explain the analysis of state machines with D Flip-Flops. [7M]

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PART –A   (14 Marks)

1. a) Write a test bench for two input XOR gate using VHDL.   [2M]

   b) Convert JK flipflop into RS flipflop.   [2M]

   c) Differentiate between VHDL and Verilog HDL.   [2M]

   d) Explain the operation of two bit comparator.   [3M]

   e) Classify shift registers.   [3M]

   f) What is package declaration in VHDL?   [2M]

PART –B   (56 Marks)

2. a) Describe the main benefit and the main drawback of TTL gates that use Schottky   [7M]
      transistors.
   b) Explain the operation of CMOS inverter circuit.   [7M]

3. a) Explain the structure of various LOOP statements in VHDL with examples.   [7M]
   b) Explain various data types available in VHDL.   [7M]

4. a) Explain about combinational multipliers.   [7M]
   b) Design a full subtractor with logic gates and write VHDL data flow program for the [7M]
      implementation of the above subtractor.

5. a) Explain the operation of a Look ahead carry generator.   [7M]
   b) Write a VHDL program for the Full Adder.   [7M]

6. a) Design a 4-bit ripple counter using four D flip-flops.   [7M]
   b) Write a VHDL program for the 4 bit universal shift register.   [7M]

7. a) Enumerate the steps to be followed in the design of clocked synchronous state- [7M]
      machine.
   b) With a neat sketch explain the operation of a Moore machine.   [7M]

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