Code No: R1631042 **R16** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, March – 2021

LINEAR IC APPLICATIONS

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1 a) What is a level translator circuit? Why it is used with the cascaded differential amplifier? [3M]
b) What is the major difference between among SSI, MSI, LSI and VLSI ICs? [2M]
c) Draw the schematic diagram of an analog multiplier using logarithmic amplifier. [2M]
d) How is an op-amp used as a sample and hold circuit? [3M]
e) List important features of the 555 timer. [2M]
f) Calculate the values of LSB, MSB and full scale output for an 8-bit DAC, if the applied input is in the range of 0-10V. [2M]

PART –B (56 Marks)

2 a) Draw the circuit diagram of a basic differential amplifier and explain its transfer characteristics. [7M]
b) Draw the circuit diagram of dual input unbalanced output differential amplifier and derive the expression for dc analysis. [7M]

3 a) Name the most important parameters of an operational amplifier. What are their ideal values and practical values? [7M]
b) Explain dominant pole frequency compensation method. [7M]

4 a) What are the advantages of instrumentation amplifier? Derive an expression for the transfer function of an instrumentation amplifier. [7M]
b) For the non-inverting a.c amplifier R_{in}=50Ω, C_i=0.1μf, R_1=100Ω, R_F=1kΩ and R_0=10kΩ. Determine the gain and bandwidth of the amplifier. [7M]

5 a) With a suitable circuit diagram, explain the operation of Narrow band pass filter (NBPF) and give the necessary design expression. [7M]
b) Design a wide band-pass filter with f_L=200 Hz. F_H=1 kHz and a pass band gain=4. Draw the frequency response and calculate 'Q' factor for the filter. [7M]

6 a) Draw the block diagram of generation of FSK using a PLL. Explain how tracking range affects error voltage in detection? [7M]
b) Underline the principle of operation of a Varactor diode and draw the circuit of a VCO using such a diode. [7M]

7 a) Define the following terms: [7M]
i) Accuracy ii) Resolution iii) Conversion time iv) Percentage resolution.
b) Draw the circuit of a ladder type DAC for 4 bits and derive expression for output voltage. [7M]

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PART –A (14 Marks)

1 a) What are the four differential amplifier configurations? Which one is not commonly used? [3M]
b) What are the three operating temperature ranges of the IC? [2M]
c) Explain the need for emitter resistor R_E in an emitter coupled astable multivibrator. [3M]
d) Draw a circuit for multiplication of two analog signals. [2M]
e) What is the major difference between digital and analog PLLs. [2M]
f) Define the parameters resolution and settling time of DAC. Obtain the value of resolution for an 8-bit DAC. [2M]

PART –B (56 Marks)

2 a) Explain the single input unbalanced output differential amplifier and derive an expression for voltage gain of this differential amplifier. [7M]
b) Write a short note on cascade differential amplifier stages with suitable circuit diagram. [7M]

3 a) Define the terms: CMRR, PSRR, SVRR, Input bias current, Input offset voltage and Gain bandwidth product. [7M]
b) If an op-amp has a slew rate of 3 V/μs, find the rise time for an output voltage of 12V amplitude resulting from a rectangular pulse input if the op-amp is slew rate limited. [7M]

4 a) What are the different modes of operation of an active integrator? Explain them. [7M]
b) Design a practical integrator circuit to process the sinusoidal input waveform up to 1KHz and the input amplitude is 10mV. Assume necessary standard values of resistance. [7M]

5 a) Draw the op-amp circuit configuration of a band-pass filter formed by cascading two pole high-pass filters and a two pole low-pass filter, and derive the expression for centre frequency f_0. [7M]
b) Describe the working of sample and hold circuit with a suitable diagram. [7M]

6 a) Draw the pin diagram of 566 VCO IC and list important specifications of 566 VCO IC. [7M]
b) Derive an expression for the lock-in range of a PLL? [7M]

7 a) Draw the block diagram of a ramp-type digital voltmeter and explain its working. [7M]
b) Describe the principle of working of an R-2R DAC. What is the minimum and maximum value of gain for it? How can a DAC be used as current-to-voltage converter? [7M]

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Code No: R1631042 **R16** SET - 3

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Time: 3 hours Max. Marks: 70

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2. Answering the question in **Part-A** is compulsory
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

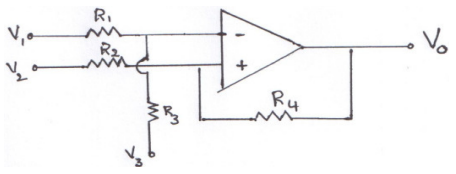
1 a) Why is a cascaded configuration used in an op-amp? [2M]
b) What are the advantages of using a schematic symbol for an op-amp? [3M]
c) Describe the operation of zero-crossing detector. [3M]
d) What is an all-pass filter? Where and why it is needed? [2M]
e) What is a capture range and lock range of PLL? [2M]
f) Define important performance specifications of Digital to Analog converters listing their typical values. [2M]

PART –B (56 Marks)

2 a) Mention the types of open loop configurations of an Op-Amp. Explain each configuration in detail. [7M]
b) Draw the ac and dc equivalent circuits of single input balanced output differential amplifier and also derive an expression for voltage gain of this differential amplifier. [7M]

3 a) Derive CMRR of emitter coupled differential amplifier. What do you mean by difference mode gain? [7M]
b) For an OP-AMP, PSRR is 70dB, CMRR is 10^5, and differential mode gain is 10^5. The output voltage changes by 20V in 4 μs. Calculate: [7M]
i) Numerical value of PSRR, ii) Common mode gain, iii) Slew rate.

4 a) Explain the operation of a practical differentiator. Use relevant expressions, diagrams. [7M]
b) In the below circuit, it can be shown that $V_0=\alpha_1V_1+\alpha_2V_2+\alpha_3V_3$. Find the values of α_1, α_2, α_3. Find the value of V_0 if [7M]
i) R_4 is Short circuited ii) R_4 is removed iii) R_1 is short circuited.



5 a) Describe the principle of operation of an inverting first order low-pass filter using op-amp and draw its frequency response curve. [7M]
b) Design a second order Butter-worth low pass filter having a cut-off frequency of 1KHz. The damping factor is equal to 1.414. [7M]

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6 a) Draw the dc voltage versus phase difference characteristics of balanced modulator phase detector of a PLL indicating all important regions. [7M]

b) With a neat functional diagram, explain the operation of VCO and also derive an expression for free running frequency, f_0. [7M]

7 a) Using a neat sketch, explain the working of a parallel comparator ADC. [7M]

b) Draw the circuit of a Weighted Resistor DAC and obtain expression for n-bits. [7M]

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2. Answering the question in **Part-A** is compulsory
3. Answer any **FOUR** Questions from **Part-B**

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PART –A **(14 Marks)**

1	a)	Explain why open-loop op-amp configuration is not used for linear applications?	[2M]
	b)	What is the difference between monolithic and hybrid ICs?	[2M]
	c)	Explain the working principle of a feedback limiter circuit.	[2M]
	d)	Define a filter. How are filters classified?	[3M]
	e)	For being used in a PLL, describe the characteristics that a VCO must possess.	[3M]
	f)	Compare Successive approximation A/D converter with Parallel comparator type A/D converter.	[2M]

PART –B **(56 Marks)**

2	a)	With suitable circuit diagram, explain about Dual input balanced output differential amplifier. And derive necessary expressions for dc and ac analysis.	[7M]
	b)	What is a differential amplifier? Mention the classification of differential amplifier with neat diagrams.	[7M]
3	a)	What is an Op-Amp? Draw the functional block diagram of an Op-Amp and explain each block in detail.	[7M]
	b)	An op-amp has a slew rate of 2V/μs. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation?	[7M]
4	a)	Using three op-amps draw the circuit diagram of an instrumentation amplifier and derive an expression for the output voltage.	[7M]
	b)	Design a single op-amp logarithmic amplifier and derive the relation between the output and input voltage? Explain why it is called a logarithmic amplifier?	[7M]
5	a)	Draw a band pass filter circuit with its frequency response curve. Explain its working.	[7M]
	b)	Using an op-amp, design a second order low-pass filter with a cutoff frequency of 1KHz.	[7M]
6	a)	Draw the circuit diagram of a 555 timer connected as an astable multivibrator and explain its operation.	[7M]
	b)	Using 555 timers, design a monostable multivibrator to produce pulses of width of 110 msec. Use a 1μF capacitor.	[7M]
7	a)	Draw and explain the block diagram of a counter type ADC and list out its disadvantages.	[7M]
	b)	Draw the simplified block diagram of a successive approximation ADC and explain its working.	[7M]

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