Code No: R1631043 **R16** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2019

DIGITAL IC APPLICATIONS

(**Common to** Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) What is fan-in and fan-out? [2M]
   b) Write down the syntax of a VHDL entity declaration. [2M]
   c) What do you mean by concurrent statement? [2M]
   d) Briefly discuss about priority encoder. [3M]
   e) What is race around condition? How it is avoided? [3M]
   f) What is timing diagram? [2M]

PART –B (56 Marks)

2. a) Which bipolar family is best suited for LSI? Show the circuit of a 4-input NAND gate using CMOS transistors. [7M]
   b) List out the family members of TTL family. Write down the typical values of characteristics of all the TTL series. [7M]

3. a) With suitable block diagram explain about the design flow of VHDL. [7M]
   b) Explain the various scalar data types supported by VHDL with suitable examples. [7M]

4. a) With suitable example, explain PROCESS statement in VHDL. [7M]
   b) List out the differences between inertial delay model and transport delay model with example. [7M]

5. a) Write a VHDL program for 16-bit barrel shifter for left circular shift only? [7M]
   b) Write a VHDL code for four bit parallel adder/subtractor. [7M]

6. a) Discuss the logic circuit of 74 x 377 register. Write a VHDL program for the same in structural style. [7M]
   b) Design a 4-bit binary synchronous counter using 74x74. [7M]

7. a) What are the Moore and Mealy machines? Compare them. [7M]
   b) For the machine given in table, find the equivalence partition and a corresponding reduced machine in standard form and also explain the procedure. [7M]

PS	NS,Z	
	X=0	X=1
A	B, 0	E, 0
B	E, 0	D, 0
C	D, 1	A, 0
D	C, 1	E, 0
E	B, 0	D, 0

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Code No: R1631043 **R16** SET - 2

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2019

DIGITAL IC APPLICATIONS

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) State the noise margin for CMOS family. [2M]
   b) List out the different operators in VHDL. [3M]
   c) What do you mean by sensitivity list? [2M]
   d) What do you mean by comparator? [2M]
   e) List out the differences between asynchronous counter and synchronous counter. [3M]
   f) What is state assignment? [2M]

PART –B (56 Marks)

2. a) Explain what is mean by logic family? Construct an Ex-NOR circuit using CMOS transistors and explain its operation. [7M]
   b) Explain the difference between current sinking and current sourcing logic circuits. How are they estimated for CMOS families? [7M]

3. a) What is package body? Explain with example. [7M]
   b) With the help of block diagram explain the program structure of VHDL. [7M]

4. a) Explain CASE statement in VHDL with example. [7M]
   b) List out the differences between variable assignment statement and signal assignment statement with example. [7M]

5. a) Design a function $F = ABC+ (A+B+C)'$ by using 74X138. [7M]
   b) Write down the behavioral VHDL architecture for fixed point to floating point conversion with rounding? [7M]

6. a) Draw the logic diagram of 74x74 IC and explain the operation. Develop the VHDL model for this IC. [7M]
   b) Write down the VHDL code for an n-bit left to right shift register. [7M]
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7. a) Explain the state equivalence and machine equivalence with reference to sequential machines. [7M]
   b) Reduce the number of states in the state table, and tabulate the reduced state table and give proper assignment. [7M]

PS	NS,Z X=0	X=1
A	F, 0	B, 0
B	D, 0	C, 0
C	F, 0	E, 0
D	G, 1	A, 0
E	D, 0	C, 0
F	F, 1	B, 1
G	G, 0	H, 0
H	G, 1	A, 0

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Code No: R1631043 **R16** SET - 3

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2019

DIGITAL IC APPLICATIONS

(**Common to** Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A **(14 Marks)**

1.	a)	What is transition time? How it is different from propagation time?	[2M]
	b)	List out the different data types in VHDL.	[3M]
	c)	What are the assignment statements in VHDL?	[2M]
	d)	What do you mean encoder?	[2M]
	e)	Draw the connection diagram for IC 7490.	[3M]
	f)	What is state table?	[2M]

PART –B **(56 Marks)**

2.	a)	Draw the circuit diagram and functional table of ECL 10K 2-input OR/NOR gate and explain its operation.	[7M]
	b)	Construct a circuit with CMOS as a driver and TTL as a load? Explain the interfacing operation.	[7M]
3.	a)	What are the various types of objects in VHDL and explain?	[7M]
	b)	What is the use of library clause and use clause? Give examples.	[7M]
4.	a)	Explain the logic synthesis process with suitable block diagram?	[7M]
	b)	Explain IF statement in VHDL with example. Give the comparisons between CASE and IF statement.	[7M]
5.	a)	What is multiplexer? Draw the logic diagram of 8 to 1 line multiplexer.	[7M]
	b)	Write a behavioral VHDL program for a dual priority encoder.	[7M]
6.	a)	Explain the operation of a 4-bit synchronous binary counter with the required diagram and waveforms.	[7M]
	b)	Write VHDL code for 4-bit serial-In Parallel-out register.	[7M]
7.	a)	With suitable example explain the Mealy and Moore models?	[7M]
	b)	Explain One hot encoding with a suitable example.	[7M]

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Code No: R1631043 **R16** SET - 4

III B. Tech I Semester Regular/Supplementary Examinations, October/November - 2019

DIGITAL IC APPLICATIONS

(**Common to** Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) Explain the difference between static and dynamic power consumption. [2M]
   b) Write the acronym for VHDL. [2M]
   c) What do you mean by sequential statements? [2M]
   d) What is decoder? [3M]
   e) Draw the pin diagram of IC 7495. [3M]
   f) What is state diagram? [2M]

PART –B (56 Marks)

2. a) What is steady-state behavior? Explain the different voltage parameters, current parameters and noise margins for CMOS devices. [7M]
   b) Analyze the fall time CMOS inverter output with R_L = 100Ω, V_L = 2:5V and C_L = 10pF. Assume V_L as stable state voltage. [7M]

3. a) What is subprogram? Give the syntax of VHDL functions. [7M]
   b) List out the differences between VHDL functions and procedures with example. [7M]

4. a) Explain the following statements with examples: [7M]
      i) IF statement ii) EXIT statement
      iii) Assert Statement iv) Report Statement.
   b) Explain the concept of Inertial Delay Model along with one example. [7M]

5. a) Design a barrel shifter for 8-bit using three control inputs. Write a VHDL program for the same in data flow style. [7M]
   b) Using a process statement write a VHDL source code for 4 to 1 multiplexer. [7M]

6. a) List the basic types of shift registers in terms of data movement with diagrams. [7M]
   b) Explain the difference between D-Latch and D-Flip flop using the process block in VHDL. [7M]

7. a) Draw the Mealy and Moore type FSM for serial adder. [7M]
   b) Write down the VHDL code for serial adder. [7M]

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