Code No: R1632043 **R16** SET - 1

III B. Tech II Semester Supplementary Examinations, April - 2021

VLSI DESIGN

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) List out few comparisons of CMOS and BI-CMOS transistors in detail. [2M]
   b) List out general observations on the design rules in detail. [2M]
   c) Explain the formal estimation of CMOS Inverter delay. [2M]
   d) What is testing? [3M]
   e) List out the applications of FPGAs. [3M]
   f) How to get Low power consumption in VLSI Design? [2M]

PART –B (56 Marks)

2. a) With a neat sketch explain BICMOS fabrication in an n-well process in detail. [7M]
   b) Explain the steps in twin-tub process of CMOS fabrication with suitable sketch. [7M]

3. a) What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate. [7M]
   b) Draw the circuit diagram of CMOS inverter and explain its operation. [7M]

4. a) Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [7M]
   b) Define standard unit capacitance? Explain. [7M]

5. a) List out different Built-In Self Test techniques used in VLSI design and explain each one in detail. [7M]
   b) Write short notes on Testable Design Techniques in detail. [7M]

6. a) Explain the concept of FPGA Implementation of Half adder along with circuit diagram. [7M]
   b) Explain the following terms: [7M]
   i) Altera Flex 10FPGA; ii) Xilinx XC4000 series FPGA.

7. Explain the concept of different Low Power CMOS Logic Circuits along with examples. [14M]

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