Code No:**R164104C** **R16** **Set No. 1**

**IV B.Tech I Semester Supplementary Examinations, February- 2020**

# SYSTEM DESIGN THROUGH VERILOG

**(Electronics and Communication Engineering)**

**Time: 3 hours** **Max. Marks: 70**

***Question paper consists of Part-A and Part-B***
***Answer ALL sub questions from Part-A***
***Answer any FOUR questions from Part-B***
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## PART–A *(14 Marks)*

| | | | |
|---|---|---|---|
| 1. | a) | Compare synthesis and simulation. | [2] |
| | b) | Draw the truth table of AND gate primitive. | [3] |
| | c) | Write the syntax of intra assignment delay. | [2] |
| | d) | Write the syntax of an AND gate in dataflow format and write its test bench. | [2] |
| | e) | What is continuous assignment synthesis? | [2] |
| | f) | Explain memory operators? | [3] |

## PART–B *(4x14 = 56 Marks)*

| | | | |
|---|---|---|---|
| 2. | a) | Write a short notes on<br>(i) strengths (ii)parameters (iii) operators (iv) system tasks | [14] |
| 3. | a) | Design all 4 types of tri state buffers, write its VERILOG code and test bench. | [7] |
| | b) | Explain design of Flip flops with gate primitives. | [7] |
| 4 | | Write the syntax of (i) for loop (ii) disable construct (iii) while loop with suitable examples and test benches. | [14] |
| 5. | a) | Design an edge triggered flip flop through continuous assignments for the gates and write its test bench. | [7] |
| | b) | Write VERILOG code for AOI gate and its test bench. | [7] |
| 6. | a) | Explain simple latch with Verilog module. | [6] |
| | b) | Design Verilog module of an edge triggered flip flop built with the latch. | [8] |
| 7. | | Write a Verilog description for SRAM and implement it. | [14] |