Code No: R1921042 **R19** SET - 1

II B. Tech I Semester Regular Examinations, March - 2021
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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1	a)	Solve i) $(AD012)_{16} = (X)_5$ ii) $(5.204)_{10} = (X)_{3.}$	[8M]
	b)	Perform the following operations using r-1`s complement arithmetic, i) $(+43)_{10} - (-53)_{10}$ ii) $(3F85)_{16} - (1E73)_{16}$.	[7M]
		Or	
2	a)	What are logic gates? Explain about different logic gates i) OR gate ii) AND gate iii) NAND gate iv) X-OR gate.	[8M]
	b)	A receiver with even parity hamming code is received the data as 1110110. Determine the correct code.	[7M]
3	a)	Prove the following expression using Boolean algebra and De-Morgan's theorems. Y′Z′+W′X′Z′+W′XY+WYZ′=Z′	[8M]
	b)	. Explain about three and four variable K-map.	[7M]
		Or	
4	a)	Write a short note on Full Adder.	[8M]
	b)	Draw the circuit diagram of a 4-bit adder-subtractor and briefly describe its functional principles.	[7M]
5	a)	Design and explain BCD to decimal decoder and draw its logic diagram.	[8M]
	b)	What is encoder? Design octal to binary encoder.	[7M]
		Or	
6	a)	Briefly describe about the programmable array logic with suitable diagrams.	[8M]
	b)	Implement the following Boolean function with a multiplexer, i) $F(A,B,C,D) = \sum(1,2,5,8,6,10,12,14)$ ii) $F(A,B,C,D) = \sum(1,2,5,6,12)$	[7M]
7	a)	Explain about types of sequential circuits.	[8M]
	b)	Conversion of SR flip-flop to T-flip-flop.	[7M]
		Or	
8	a)	Draw and explain the logic diagram for a 4-bit binary ripple down counter using positive edge triggered flip-flops.	[8M]
	b)	Explain the Buffer Register and Control Buffer Register.	[7M]
9	a)	Explain about State diagram and State table in sequential circuits.	[8M]
	b)	Discuss the realization of sequence generator with diagram.	[7M]
		Or	
10	a)	Draw state diagrams of a sequence detector which can detect 110.	
	b)	Draw and explain Moore circuit.	
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Code No: R1921042 **R19** SET - 2

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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions each Question from each unit
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1	a)	Deduce X from the following. i) $(BA0.C)_{16} = (X)_8$ ii) $(10101100)_2 = (X)_{16}$. iii) $(FFE.C) = (X)_2$	[8M]
	b)	What is an excess-3 BCD code? Which short coming of the 8421 BCD code is overcome in the excess-3 BCD code? Illustrate with the help of an example.	[7M]
		Or	
2	a)	Explain exclusive OR (EX-OR) and exclusive-NOR (EX-NOR) logic gates with truth tables.	[8M]
	b)	Generate Hamming code for the given 11 bit message 10101110101 and rewrite the entire message with Hamming code.	[7M]
3	a)	Find the compliments of the following, i) (AB′+C)D′+E. ii) (ABC)′(A+B+C). iii) AB′C+A′BC+ABC.	[8M]
	b)	Simplify the function using six variable K-map F(A,B,C,D,E,F)=∑m(0,5,7,8,9,12,13,23,24,25,28,29,37,55,56,57,60,61).	[7M]
		Or	
4	a)	Write a short note on Half subtractor.	[8M]
	b)	Draw the logic diagram of a three-digit Excess-3 adder? And briefly describe its functional principle.	[7M]
5	a)	What is decoder? Construct 3*8 decoder using logic gates and truth table.	[8M]
	b)	Design 8*1 multiplexer using 2*1 multiplexer.	[7M]
		Or	
6	a)	Briefly describe about the programmable logic arrays with suitable diagrams.	[8M]
	b)	Design full adder from 3 to 8 decoder.	[7M]
7	a)	What do you mean by triggering? Explain the various triggering modes with examples.	[8M]
	b)	Convert T flip-flop to D flip-flop.	[7M]
		Or	
8	a)	Design a modulo-12 up synchronous counter using T-flip flops and draw the circuit diagram.	[8M]
	b)	Explain in detail about shift registers.	[7M]
9	a)	Explain state transition function, finite state model, Terminal state and strongly connected machine in finite state machine.	[8M]
	b)	Explain the state reduction technique.	[7M]
		Or	
10	a)	Draw state diagrams of a sequence detector which can detect 010.	[8M]
	b)	Draw the diagram of Mealy type FSM for serial adder.	[7M]
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Code No: R1921042 **R19** SET - 3

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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions each Question from each unit
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1	a)	Discuss about the representation of negative number.	[8M]
	b)	Explain BCD, excess-3 and gray codes with examples.	[7M]
		Or	
2	a)	What are SOP and POS forms of logical functions? Explain the standard or canonical SOP and POS forms.	[8M]
	b)	State the Boolean algebra postulates and explain in detail with examples.	[7M]
3	a)	Simplify the following Boolean expression to a minimum number of literals, i) X′Y′+XY+X′Y. ii) (X+Y) (X+Y′). iii) X′+XY+XZ′+XY′Z′	[8M]
	b)	Explain in detail about five and six variable K-map.	[7M]
		Or	
4	a)	Implement the NOR gate realization of full adder.	[8M]
	b)	Explain the operation of carry look-a-head adder.	[7M]
5	a)	Differentiate Demultiplexer and Decoder.	[8M]
	b)	Define multiplexer and explain the procedure to implement 32*1 MUX by using 4*1 multiplexers.	[7M]
		Or	
6	a)	Write the comparisons between ROM and PLA.	[8M]
	b)	Explain briefly about seven segment displays.	[7M]
7	a)	Explain the operation of D-flip flop with the help of truth table.	[8M]
	b)	Explain the basic principles of ripple counter.	[7M]
		Or	
8	a)	Design a Mod-6 synchronous counter using J-K flip flops.	[8M]
	b)	Draw and explain the working of shift right register.	[7M]
9	a)	Explain the analysis of clocked sequential circuits.	[8M]
	b)	Implement the Sequential Circuit with clock to detect the given sequence without overlapping.	[7M]
		Or	
10	a)	Draw state diagrams of a sequence detector which can detect 011.	[8M]
	b)	Explain the state machine capabilities and limitations in detail.	[7M]
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1 a) Explain the complement representation of negative number with examples. [8M]

b) Define even and odd parity. With the help of the generalized form of the Hamming code, explain how the number of parity bits required to transmit a given number of data bits. [7M]

Or

2 a) Write canonical sum and product for each of the following logic functions, [8M]
i) $F=\sum_{x,y}(1,3)$ ii) F = A+B.C iii) $F = \pi_{x,y,z}(0,6,7)$

b) Perform the realization of all basic logic gates using universal gates. [7M]

3 a) Simplify the following to least number of literals by manipulation of Boolean algebra. [8M]
i) AB′C′D+A′B′D+BCD′+A′B+BC′.
ii) ABC+A′B+ABC′.
iii) X+XYZ+X′YZ+XW+XW′+X′Y.

b) Minimize the following function using the Quine-McCluskey method. [7M]
$Y=\sum(1,2,5,8,9,10,12,13,16,18,24,25,26,28,29,31)$

Or

4 a) Design 1-bit full adder using two half adders. Draw the logic diagram with its truth table. [8M]

b) Design a 4-bit carry ahead adder circuit. [7M]

5 a) Design a 1:8 demultiplexer using two 1:4 demultiplexer. [8M]

b) Implement a 64:1 MUX using 16:1 and 4:1 Muxs. [7M]

Or

6 a) List the merits and demerits of PROM ,PAL and PLA. [8M]

b) Implement $f(A,B,C,D) = \sum(0,1,3,5,6,8,9,11,12,13)$ using 8:1 MUX and explain its procedure. [7M]

7 a) Explain about master-slave flip-flop in detail. [8M]

b) Design a 4-bit ripple counter using T-flip-flop. Explain using waveforms. [7M]

Or

8 a) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams. [8M]

b) Draw a 4-bit bi-directional shift register logic diagram and explain its operation. [7M]

9 a) Explain the difference among a truth table, a state table, a characteristic table and an excitation table. [8M]

b) Draw state diagrams of a sequence detector which can detect 101. [7M]

Or

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10 a) Explain in detail the Mealy state diagram with one example. [8M]

b) Design the Clocked Sequential Circuit to detect the given sequence with overlapping. [7M]