Code No: R1921042 **R19** SET - 1

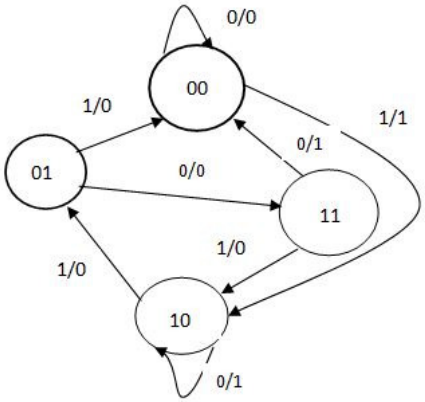
II B. Tech I Semester Supplementary Examinations, September - 2021
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~~

1	a)	Add the following numbers using the 2's complement method. (i) +49 and -37 (ii)-48 and +31	[6M]
	b)	Given the 8 bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors.	[7M]
	c)	Convert the binary number $(101111.1101)_2$ into its decimal equivalent.	[2M]
		Or	
2	a)	Explain Demorgan's theorems in Boolean Algebra.	[6M]
	b)	Implement EX OR gate using only four two input NAND gates.	[4M]
	c)	Convert the Boolean function F(A,B,C,D) = A+BC+ACD into standard POS form.	[5M]
3	a)	Minimize the following expression using Quine-McCluskey method $Y = \bar{A}\ B\ \bar{C}\ \bar{D} + \bar{A}\ B\ \bar{C}\ D + A\ B\ \bar{C}\ \bar{D} + A\ B\ \bar{C}\ D + A\ \bar{B}\ \bar{C}\ D + \bar{A}\ \bar{B}\ C\ \bar{D}$	[12M]
	b)	What are the advantages and disadvantages of K-map?	[3M]
		Or	
4	a)	Implement full adder using decoder and OR gates	[5M]
	b)	Design a 4-bit BCD to gray code converter and draw its logic diagram.	[10M]
5	a)	Define an encoder. Design octal to binary encoder	[10M]
	b)	List the applications of multiplexers.	[3M]
	c)	What is a magnitude comparator?	[2M]
		Or	
6	a)	Design a combinational circuit using PROM that accepts 3-bit binary number and generates its equivalent excess-3 code.	[10M]
	b)	Compare the three combinational PLDs – PROM, PLA and PAL.	[5M]
7	a)	Differentiate between synchronous and asynchronous counters.	[4M]
	b)	What is a shift register? Name the different types of shift registers.	[4M]
	c)	Explain the operation of the bi-directional shift register.	[7M]
		Or	
8	a)	Convert a J-K flip-flop into a T type flip-flop.	[10M]
	b)	Discuss the effects of propagation delay in ripple counters.	[5M]
~~~~~~~~~~~~~~~~~~~~~~~~~

9 a) A sequential circuit has one input and one output .The state diagram is shown below. Design the sequential circuit with D flip-flops. [9M]



b) Discuss the capabilities and limitations of Finite State Machines. [6M]

Or

10 a) Reduce the state table using partition technique. [10M]

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

b) Distinguish Mealy and Moore machines. [5M]