SIR C.R.REDDY COLLEGE OF ENGINEERING, ELURU

DEPARTMENT OF INFORMATION TECHNOLOGY

LESSON PLAN

SUBJECT: DIGITAL LOGIC DESIGN

CLASS: 2/4 B.Tech. I SEMESTER, A.Y.2019-20

INSTRUCTOR: Sri A.M.K.KANNA BABU

SIR C R REDDY COLLEGE OF ENGINEERING
DEPARTMENT OF INFORMATION TECHNOLOGY

PROGRAMME : B. Tech.
SEMESTER : II/IV I Semester
A.YEAR : 2019-20

COURSE : DIGITAL LOGIC DESIGN

INSTRUCTOR : Sri A.M.K.KANNA BABU

Course Contents

Category of Course	Course Title	Course Code	Credits- 4	Theory Paper
Departmental Core	DIGITAL LOGIC DESIGN	R1621053	L-3 T-1	Max.Marks-70 Duration-3hrs.

Course description:

This course on 'Digital Logic Design' presents a logical treatment of all the fundamental concepts necessary to understand the design of a computer. It is designed to cover the requirements of a first-course in computer organization. This course starts with the foundation material on data representation, computer arithmetic's, combinatorial and sequential circuit design. These are followed by a description of the general features of memory systems

Course objectives:

1. To introduce number systems and Binary codes.
2. To introduce basic postulates of Boolean algebra and shows the correlation between Boolean Expressions and Boolean functions.
3. To introduce the methods for simplifying Boolean expressions.
4. To outline the formal procedures for the analysis and design of combinational circuits and Sequential circuits.

Students who have successfully completed this course will have full understanding of the following concepts

Course Outcomes for Digital Logic Design:

- Able to understand Binary Systems, Boolean Functions, Logic Gates, Combinational Circuits and Sequential Circuits.
- Able to apply number systems, Boolean functions and logic gates for the design of logic circuits.
- Able to analyze different combinational and sequential circuits.
- Able to design different combinational and sequential circuits.

Online References:

www.electronics-tutorials.ws
https://www.cse.iitb.ac.in/~supratik/courses/cs226

Prerequisite:

Students are expected to know mathematical fundamental and logical skills.

Internal Assessment Details:

Internal Test 1& 2	: 15 Marks
Online Test 1 & 2	: 10 Marks
Assignment-1 & 2	: 5 Marks
Total	: 30 Marks

II Year - I Semester

L	T	P	C
4	0	0	3

DIGITAL LOGIC DESIGN

OBJECTIVE:

To introduce the basic tools for design with combinational and sequential digital logic and state machines.

To learn simple digital circuits in preparation for computer engineering.

UNIT- I: Digital Systems and Binary Numbers

Digital Systems, Binary Numbers, Binary Numbers, Octal and Hexadecimal Numbers, Complements of Numbers, Complements of Numbers, Signed Binary Numbers, Arithmetic addition and subtraction

UNIT -II: Concept of Boolean algebra

Basic Theorems and Properties of Boolean algebra, Boolean Functions, Canonical and Standard Forms, Minterms and Maxterms,

UNIT- III: Gate level Minimization

Map Method, Two-Variable K-Map, Three-Variable K-Map, Four Variable K-Maps. Products of Sum Simplification, Sum of Products Simplification, Don't – Care Conditions, NAND and NOR Implementation, Exclusive-OR Function

UNIT- IV: Combinational Logic

Introduction, Analysis Procedure, Design Procedure, Binary Adder–Subtractor, Decimal Adder, Binary Multiplier, Decoders, Encoders, Multiplexers, HDL Models of Combinational Circuits

UNIT- V: Synchronous Sequential Logic

Introduction to Sequential Circuits, Storage Elements: Latches, Storage Elements: Flip-Flops, Analysis of Clocked **Sequential** Circuits, Mealy and Moore Models of Finite State Machines

UNIT -VI: Registers and Counters

Registers, Shift Registers, Ripple Counters, Synchronous Counters, Ring Counter, Johnson Counter, Ripple Counter

TEXT BOOKS:

Digital Design, 5/e, M.Morris Mano, Michael D Ciletti, PEA.
Fundamentals of Logic Design, 5/e, Roth, Cengage.

REFERENCE BOOKS:

Digital Logic and Computer Design, M.Morris Mano, PEA.
Digital Logic Design, Leach, Malvino, Saha, TMH.
Modern Digital Electronics, R.P. Jain, TMH.

COURSE SCHEDULE

The schedule for the whole course/subject is:

Unit No	Description of the Chapter	Description of the Topics	Total no of periods (L+T)
1	Binary Systems	Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Binary Numbers. Binary Codes. Binary Storage and Registers. Binary Logic.	10
2	Boolean algebra and Logic Gates	Basic Definitions. Axiomatic Definition of Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits.	10
3	Combinational Logic Design, Gate-Level Minimization	The Map Method. Four-Variable Map. Five-Variable Map. Product of Sums Simplification. Don't-Care Conditions. NAND and NOR Implementation. Other Two- Level Implementations.	10

		Exclusive-OR Function. Hardware Description Language (HDL).	
4	Combinational Logic	Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder- Subtractor. Decimal Adder. Binary Multiplier. Magnitude Comparator. Decoders. Encoders. Multiplexers. HDL For Combinational Circuits.	10
5	Sequential Logic Design, Synchronous Sequential Logic	Sequential Circuits. Latches. Flip-Flops. Analysis of Clocked Sequential Circuits. HDL For Sequential Circuits. State Reduction and Assignment. Design Procedure.	10
6.	Registers and Counters.	Registers. Shift Registers. Ripple Counters. Synchronous Counters. Other Counters. HDL for Registers and Counters.	10

Total number of estimated periods : 60 periods

Signature of the H.O.D

Signature of the Faculty

Date:

LECTURE PLAN

Sl.No	Topics to be covered	No. of Lecture	Teaching method	Program Outcomes
1.	Introduction to Digital Systems, Binary numbers	1	BB	a,c
2.	Number system conversion, Octal and Hexadecimal Numbers	1	BB	a,b,c
3.	Complements	1	BB	b,c,d
4.	Signed Binary Numbers	1	BB	b,c,d
5.	Binary Codes	1	BB	b,c,d
6.	Binary multiplication and division	1	BB	b,c,d
7.	BCD addition and subtraction	1	BB	b,c,d
8.	Gray Code and parity bits	1	BB	b,c,d
9.	ASCII,EBCDIC, Binary Storage and Registers	1	PPT with LCD	b,c,d
10.	Binary Logic gates	1	BB	b,c,d
11.	Axiomatic Definition of Boolean Algebra	1	BB	b,c,d
12.	Boolean Functions	2	BB	b,c,d
13.	SOP and POS	1	BB	b,c,d
14.	Standard Forms	1	BB	b,c,d
15.	Conversion of one canonical to another	2	BB	b,c,d
16.	Reduce the Boolean functions	1	BB	b,c,d
17.	Other Logic Operations	1	BB	b,c,d
18.	Digital Logic Gates	1	BB	b,c,d
19.	The Map Method	1	PPT with LCD	b,c,d
20.	Three variable map	1	BB	b,c,d
21.	Four-Variable Map	2	BB	b,c,d
22.	Five-Variable Map	1	BB	b,c,d
23.	Product of Sums Simplification	1	BB	b,c,d
24.	Tabulation method	1	BB	b,c,d
25.	NAND and NOR , Other Two- Level Implementations Implementation	1	BB	b,c,d

26.	Exclusive-OR Function	1	BB	b,c,d
27.	Hardware Description Language (HDL)	1	BB	b,c,d
28.	Combinational Circuits Analysis Procedure	1	BB	b,c,d
29.	Design Procedure	1	BB	b,c,d
30.	Half adder, Full adder, Half subtractor and Full subtractor	2	BB	b,c,d
31.	Binary Adder- Subtractor	1	PPT with LCD	b,c,d
32.	Decimal Adder	1		b,c,d
33.	Binary Multiplier	1	BB	b,c,d
34.	Magnitude Comparator	1	BB	b,c,d
35.	Decoders, Encoders	1	BB	b,c,d
36.	Multiplexers, Priority Encoder	1	BB	b,c,d
37.	Sequential Circuits	1	BB	b,c,d
38.	Latches	2	BB	b,c,d
39.	Flip-Flops	2	BB	b,c,d
40.	Analysis of Clocked Sequential Circuits	2	BB	b,c,d
41.	Design of a sequential circuits	2	BB	b,c,d
42.	State Reduction and Assignment	1	BB	b,c,d
43.	Registers	1	BB	b,c,d
44.	Shift register	2	BB	b,c,d
45.	Universal shift register	1	BB	b,c,d
46.	counter	1	BB	b,c,d
47.	Ripple counter	1	BB	b,c,d
48.	Synchronous counter	2	BB	b,c,d
49.	Other counters	2	BB	b,c,d

Total number of estimated periods : 60 periods

Short and essay questions unit wise

UNIT-I

1. Find the two's complements of following numbers:
   a) $(1230)_4$ and $(23)_4$ b) $(135.4)_6$ and c) $(43.2)_6$
2. Convert the following numbers from the given base to the base indicated.
   a) Decimal 225.225 to binary, octal and hexadecimal.
   b) Binary (11010111.110) to decimal, octal and hexadecimal;
3. Convert the following numbers from the given base to the base indicated.
   (a) Octal 623.77 to decimal, binary and hexadecimal
   (b) Hexadecimal 2ACD.5 to decimal, binary and octal.
4. Convert the following number to decimal
   a) $(0.342)_6$ b) $(8.3)_9$ c) $(198)_{12}$ d) $(50)_7$
5. Obtain the 9's and 10's complement of the following decimal numbers
   (a) 13579 b) 09900 c) 10000 d) 00000 e) 90090
6. Obtain the 1's and 2's complement of the following binary numbers
   a) 1010101 b) 0111000 c) 0000001 d) 10000 e) 00000
7. Perform the subtraction with the following numbers using 2's and 1's complement
   a) 11010.1101 – 10010.10011 b) 11010.10000 – 100.110000
8. Explain
   (a) self-complementary codes with examples.
   (b) Error-detection codes and Reflected Code
9. Explain
   a) BCD codes
   b) Register transfer with a neat diagram.
10. Explain basic logic gates with truth tables and gates
11. The decimal 17 is equal to the binary number
    a) 10010 (b) 11000 (c) 10001 (d) 01001
12. The sum of 11010 + 01111 equals
    (a) 101001 (b) 101010 (c) 110101 (d) 101000
13. The difference of 110 – 010 equals
    (a) 001 (b) 010 (c) 101 (d) 100
14. The 1's complement of 10111001 is
    (a) 01000111 (b) 01000110 (c) 11000110 (d) 10101010
15. The 2's complement of 11001000 is
    (a) 00110111 (b) 00110001 (c) 01001000 (d) 00111000
16. The binary number 10110011001010100001 can be written in octal as
    (a) 54712308 (b) 54712418(c) 26345218 (d) 231625018
17. The binary number 10001101010001101111 can be written in hexadecimal as
    (a)AD46716 (b) 8C46F16 (c) 8D46F16 (d) AE46F16
18. The BCD number for decimal 473 is
    (a) 111011010 (b) 1110111110101001 (c) 010001110011 (d) 010011110011
19. An inverter performs an operation known as
    (a) Complementation (b) assertion
    (b) Inversion (d) both answers (a) and (c)

20. The output of gate is LOW when at least one of its inputs is HIGH. It is true for
    (a) AND (b) NAND (c) OR (d) NOR
21. The output of gate is HIGH when at least one of its inputs is LOW. It is true for
    (a) AND (b) OR (c) NAND (d) NOR
22. The output of a gate is HIGH if and only if all its inputs are HIGH. It is true for
    (a)XOR (b) AND (c) OR (d) NAND
23. The output of a gate is LOW if and only if all its inputs are HIGH. It is true for
    (a)AND (b) XNOR (c) NOR (d) NAND
24. Which of the following gates cannot be used as an inverter?
    (a)NAND (b) AND (c) NOR (d) None of the above
25. The complement of a variable is always
    (a) 0 (b) 1 (c) equal to the variable (d) the inverse of the variable

UNIT-II

1. Define Boolean algebra and prove the following theorems
   i) X + X = X b) X.0 = 0 c) X + XY = X d) $(XY)^1 = X^{1+}Y^1$
2. Convert the following Boolean function into standard product of
   i. maxterms form and standard sum of minterms.
   ii. F = A'B+C+B'D'
3. Simplify the Boolean expressions to minimum number of literals
   i) **(**A + B)(A + C')(B' + C') ii) AB + (AC)' + AB'C(AB + C) iii) (A+B)' (A'+B')'
4. Simplify the Boolean expressions to minimum number of literals
   i) X' + XY + X Z' + XYZ' ii) (X+Y) (X+Y')
5. Obtain the Complement of Boolean Expression
   i) A+B+A'B'C ii) AB + A (B +C) + B'(B+D)
6. Convert the following to canonical forms
   i) F(x,y,z,w)=∑(1,3,7,9,11,12) ii) F(A,B,C) = π (0,3,6,7
7. Convert the given expression in standard POS form Y= A.(A+B+C)
8. Prove that the sum of all minterms of Boolean function for three variable is 1
9. Show that the dual of the Ex-or is equal to its complement?
10. Obtain the dual of the following Boolean Expressions
    i) AB'C+AB'D+AB' ii)A'B'C'+ABC'+A'B'C'D
11. Obtain the truth table for the function F=xy+xy'+y'z and design the circuit
12. . Expand the following Boolean expression to minterms and maxterms
    A+BC'+ABD'+ABCD
13. If F1 = Π 3,4,7,8,11,14,15 and F2 = Σ1,2,4,5,7,8,10,11,12,15 obtain minimal SOP expression for F1 • F 2 and draw the circuit using NAND gates.

UNIT-III

1. Draw the two -level NAND circuit for the following Boolean - expression:
   AB + CD E + BC (A + B) also obtain minimal SOP expression and draw the circuit using NAND gates.
2. If F1(A,B,C) = A _ B _ C F2 (A,B,C) = A_C _B Show that F1 = F2
3. Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND -NAND form.
   f (A,B,C,D) = (A + C + D) (A + B + D)(A + B + C1)(A + B + D)(A1 + B + D)
4. Implement the following Boolean function F using the two - level form:
   i. NAND-AND
   ii. AND-NOR F (A,B,C,D) = _0, 1, 2, 3, 4, 8, 9, 12
5. Simplify the following Boolean expression using K-MAP and implement using NAND gates
   F(W,X,Y,Z) = XZ+WXY+WYZ+WXZ
6. Simplify the Boolean expression using K-MAP
   F(A,B,C,D) = ∑m(1,2,3,8,9,10,11,14) +d(7,15
7. Simplify the Boolean expression using K-map and implement using NOR gates
   F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14)
8. Reduce the expression f(x,y,z,w)= πM(0,2,7,8,9,10,11,15) +d (3,4) using K-Map?
9. Simplify the Boolean expression using K-map
   F(A,B,C,D,E)= ∑m(0,1,4,5,16,17,21,25,29)
10. Simplify the Boolean expression using tabulation method
    F(A,B,C,D)= = ∑m(0,5,7,8,9,10,11,14,15)
11. Implement the Boolean function F(A,B,C,D)= A'B'+C'D'+B'C' using the following two level gates i) NAND-AND ii) NOR-OR
12. Reduce the expression using K-Map
    F(x,y,z,w)= x(y+z') (x+y') (y+z+w')
13. Simplify the Boolean expression using K-MAP
    F(A,B,C,D) = πM (3,5,6,7,11,13,14,15) +d(9,10,12)

UNIT-IV

1. Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer.
   (Use only block diagram).
2. A combinational logic circuit is defined by the following Boolean functions.
   F1 = ABC + AC F2 = ABC + AB F3 = ABC + AB
3. Design the circuit with a decoder and external gates. xy + x (wz + wz').
4. Implement the following Boolean function using 8:1 multiplexer
   F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD
5. Explain about Full Adder?
6. Explain about 2-bit Magnitude Comparator?
7. Explain Full binay subtractor in detail?
8. Design the combinational circuit binary to gray code?
9. Explain about Binary Multiplier ?
10. Implement the following Boolean function using 8:1 multiplexer
    F(A,B,C.D) = Σ (0,1,2,5,7,8,9,14,15)

11. Explain about Decimal Adder?
12. Design a 4 bit adder-subtractor circuit and explain the operation in detail?
13. Explain the functionality of a Multiplexer?
14. Design a 4 bit binary parallel subtractor and the explain operation in detail?
15. Design the combinational circuit of Binary to Excess-3 code convertors?
16. Design A Full Adder with using two half adder .
17. Implement the given function in 4:1 mux f= $\sum$m(0,1,3,5,8)
18. Design a half adder using NAND – NAND logic

UNIT-V

1. What is a flip-flop?
2. What is a latch?
3. What is a sequential circuit?
4. What is asynchronous sequential circuit?
5. Draw and explain the logic diagram of a master-slave D flip-flop using NAND gates.
6. Reduce the number of states in the state table listed below. Use an implication table.

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	0	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

7. Explain the Logic diagram of JK flip-flop?
8. Write difference between Combinational & Sequential circuits?
9. Explain the Logic diagram of SR flip-flop?
10. Draw and explain the operation of D Flip-Flop?
11. Draw and explain the operation of T Flip-Flop?

UNIT-VI

1. Design and draw the 3 bit up-down synchronous counter?
2. Explain about Shift Registers?
3. Explain about Ring counter?
4. Explain about ripple counter?
5. Explain the design of a 4 bit binary counter with parallel load in detail?
6. Design a synchronous BCD counter with JK flip-flops.

7. Design a shift register with parallel load that operates according to the following
8. function table:

9. Shift	10. Load	11. Register Operation
12. 0	13. 0	14. No Change
15. 0	16. 1	17. Load Parallel Data
18. 1	19. X	20. Shift Right

9. Design a 4-bit ring counter using T- flip flops and draw the circuit diagram and timing diagrams.
10. Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram.
11. Design a MOD-10 synchronous counter using JK flip flops