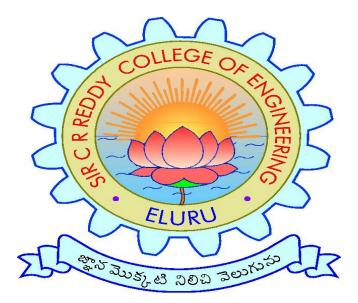
SIR C.R.REDDY COLLEGE OF ENGINEERING, ELURU DEPARTMENT OF INFORMATION TECHNOLOGY LESSON PLAN



SUBJECT: CSE 4.1.1 EMBEDDED SYSTEMS

CLASS: 4/4 B.Tech., I SEMESTER, A.Y.2019-20 INSTRUCTOR: T. Satya Nagamani

Sir C R Reddy College of Engineering DEPT. OF INFORMATION TECHNOLOGY

Course Description:

This is a graduate course surveying topics in Embedded systems. It covers basic need of Embedded systems and features and working of them, Microprocessors role in embedded systems and their functionality with the operating systems loaded with and semaphores and RTOS functionality and debugging tools and techniques.

This course builds upon the topics covered in undergraduate operating systems course, such as process synchronization, inter process communication, and Semaphores, other topics such as Microprocessor working, bus configuration, interfacing, interrupts and handling. After a brief review, these topics are studied in the context of embedded systems.

Scope and objectives :

This course is built on the student's background in Embedded systems. It covers some basic perspectives of Operating Systems, Microprocessors and Programming concepts also. Incorporates and anticipates the major developments in Embedded systems.

Prerequisite:

Students are expected to know and understand the fundamentals of microprocessors, operating systems, basic programming languages as taught in an undergraduate course using a text such as Embedded Software Primer by David.E.Simon, Operating System Concepts by Silberschatz & Galvin, Mastering C by Venugopal, OOAD by E.Bala Guruswamy. Topics should include basics of microprocessors and interrupt handling covered by microprocessor, design and implementation of operating systems, file systems, and programming concepts.

IV Year - I Semester`

Embedded Systems

Introduction to Embedded systems hardware needs; typical and advanced, timing diagrams, memories (RAM, ROM, and EPROM). Tri state devices, Buses, DMA, UART and PLD's. Built-ins on the microprocessor.

Interrupts basics, ISR; Context saving, shared data problem. Atomic and critical section, Interrupt latency.

Survey of software architectures, Round Robin, Function queue scheduling architecture, Use of real time operating systems.

RTOS, Tasks, Scheduler, Shared data reentrancy, priority inversion, mutex binary semaphore and counting semaphore.

Inter task communication, message queue, mailboxes and pipes, timer functions, events. Interrupt routines in an RTOS environment.

Embedded system software design using an RTOS. Hard real time and soft real time systems principles, Task division, need of interrupt routines, shared data.

Embedded software development tools. Host and target systems, cross compilers, linkers, locators for embedded systems. Getting embedded software into the target systems.

Debugging techniques. Testing on host machine, instruction set emulators, logic analyzers. In-circuit emulators and monitors.

Prerequisite

Operating systems, Microprocessors, Computer Organization and Electronic Devices

Internal Assessment Details:

The Assessment of a student's performance shall be evaluated as suggested below:

- For theory subjects the distribution shall be 30 marks for Internal Evaluation And 70 marks for the End Examinations.
- 2. Out of 30 internal marks, the division shall be as shown below:
- internal i & internal ii 2/3 rd of obtained marks plus assignment marks gives total 30 marks
- each assignment carries 10 marks
- take average of two internals
 Total: 30 Marks

SIR C R REDDY COLLEGE OF ENGINEERING:: ELURU DEPARTMENT OF INFORMATION TECHNOLOGY <u>COURSE SCHEDULE</u>

The schedule for the whole course/subject is:

Unit	InitDescription of the ChapterDescription of the Topics		Total no of periods
No			(L+T)
To Identify have a first look at Embedded Systems and some examples of Embedded systemsIntroduction, I1systems		Introduction, Examples of ES	8+2
2	Typical Hardware needs	Hardware needed by Embedded systems other than normal desktop systems.	12
3	Hardware Fundamentals for the software engineer.	Terminology Gates Other basic information regarding hardware devices Timing diagrams Memory	4+2
4	Advanced Hardware Fundamentals	Microprocessors Buses Direct Memory Access Interrupts Other common parts like PAL, UART Built-ins on microprocessor	4+2
5	Interrupts basics	Microprocessor Architecture Interrupt Basics like ISR and	3

		context saving	
6	The Shared Data Problem	Atomic and Critical Section	2+2
7	Interrupt Latency	Interrupt Latency in Embedded Systems	1+1
8	Survey of Software architectures Round Robin architecture 8 Round Robin With Interrupts Architecture 8 Function-queue Scheduling Architecture Real-Time Operating systems		2+1
9	Selecting an Architecture	Architecture Tips to be followed in selecting an architecture	2
10	Introduction to Real-Time Operating Systems	Tasks and Task States Tasks and Data	2
11	Shared data reentrancy and Semaphores	Semaphores and Shared Data	5+3
12	Intertask communication	Message Queues, Mail boxes and Pipes	3+2
13	Timer Functions	Timer Functions	1
14	Events	Events	2
15	Introduction to 8051 architecture	Microcontrollers Vs Microprocessors, architecture of 8051 microcontroller and programming model, registers	3+2
16	Instruction set	Instruction set of 8051	1
17	Programming	Different AL programs of 8051	2
15	Basic Design using RTOS	Overview	2+1

	Hard RTOS and soft RTOS principles, Task Division, need of Interrupts	Principles	
16	Embedded software development tools	Host and Target Machines Cross Compilers	3+2
17	Linkers, Locators for Embedded Systems	Linker/Locators for Embedded Software	2
18	Getting Embedded software onto the Target system	Getting Embedded software into the target system	3+2
19	Debugging Techniques	Testing on your Host Machine Instruction Set Simulators, Logic Analyzers, In-circuit Emulators ,Monitors	3+1
20	IOT introduction	History, architecture,M2M,Web of things	2
21	IOT communication	Protocols, layering architecture	1

Total no of instructional periods available for the course	e :	95 periods
Total no of estimated periods	:	70 periods

Signature of the H.O.D

Signature of the Faculty Date:

	LECTURE PLAN
DEPARTMET	INFORMATION TECHNOLOGY
NAME OF LECTURER	T. Satya Nagamani

Expected (Planed) date of completion of the course:

Unit Number:1 30 th June 2019
Unit Number: 2 15 th July 2019
Unit Number: 3 30 th July 2019
Unit Number: 4 15 th August 2019
Unit Number: 5 2 nd September 2019
Unit Number: 6 25th September 2019

Sl.No	Topics to be covered	No. of Lecture hours	Teaching method	Text book	CO Mapping
	UNIT-1	I	1	1	
1	Introduction, Examples of ES	8+2	BB	TB1	
2	Hardware needed by Embedded systems other than normal desktop systems.	12	BB	TB1	
3	Terminology Gates Other basic information regarding hardware devices Timing diagrams Memory	4+2	PPT with LCD	TB1	
4	Microprocessors Buses Direct Memory Access	4+2	BB	TB1	

Interrupt Basics like ISR and context saving3LCD6Atomic and Critical Section2+2BBTB16Atomic and Critical Section2+2BBTB17Interrupt Latency in Embedded Systems1+1BBTB18Microcontrollers Vs Microprocessors, architecture of 8051 microcontroller and programming model, registers3+2BBTB29Instruction set of 80511BBTB21010Different AL programs of 80512BBTB210UNIT-2PRound Robin architecture Function-queue Scheduling Architecture2+1BBTB19Round Robin With Interrupts Architecture2+1BBTB19Round Robin With Interrupts Architecture2+1BITB19Round Robin With Interrupts Architecture2+1Achitecture9Real-Time Operating systems Architecture2+1Achitecture		Interrupts				
5 Microprocessor Architecture Interrupt Basics like ISR and context saving PPT with LCD TB1 6 Atomic and Critical Section 2+2 BB TB1 7 Interrupt Latency in Embedded Systems 1+1 BB TB1 8 Microcontrollers Vs Microprocessors, architecture of 8051 microcontroller and programming model, registers 3+2 BB TB2 9 Instruction set of 8051 1 BB TB2 10 Different AL programs of 8051 2 BB TB1 VUNIT-2 9 Round Robin architecture Architecture 2+1 BB TB1 9 Round Robin with Interrupts Architecture 2+1 BB TB1 9 Round Robin With Interrupts Architecture 2+1 BI TB1 10 Tips to be followed in selecting an Architecture 2 PPT with LCD TB1		Other common parts like PAL, UART				
Interrupt Basics like ISR and context saving3LCD6Atomic and Critical Section2+2BBTB17Interrupt Latency in Embedded Systems1+1BBTB18Microcontrollers Vs Microprocessors, architecture of 8051 microcontroller and programming model, registers3+2BBTB29Instruction set of 80511BBTB21010Different AL programs of 80512BBTB210UNIT-29Round Robin architecture Function-queue Scheduling Architecture9Round Robin With Interrupts Architecture Real-Time Operating systems Architecture2+1BBTB110Tips to be followed in selecting an architecture2PPT with LCDTB1		Built-ins on microprocessor				
7 Interrupt Latency in Embedded Systems 1+1 BB TB1 8 Microcontrollers Vs Microprocessors, architecture of 8051 microcontroller and programming model, registers 3+2 BB TB2 9 Instruction set of 8051 1 BB TB2 10 Different AL programs of 8051 2 BB TB2 Actual date of completion: End Remarks: UNIT-2 9 Round Robin architecture Function-queue Scheduling Architecture 2+1 BB TB1 9 Round Robin With Interrupts Architecture 2+1 BB TB1 10 Tips to be followed in selecting an Architecture 2 PPT with LCD TB1	5	Interrupt Basics like ISR and context	3		TB1	
Systems 1+1 Image: Systems 1+1 8 Microcontrollers Vs Microprocessors, architecture of 8051 microcontroller and programming model, registers 3+2 BB TB2 9 Instruction set of 8051 1 BB TB2 10 Different AL programs of 8051 2 BB TB2 Actual date of completion: Remarks: Image: Systems Image: Systems VIIT-2 9 Round Robin architecture BB TB1 9 Round Robin with Interrupts Architecture 2+1 BB TB1 9 Round Robin with Interrupts Architecture 2+1 Image: Systems Architecture Image: Systems Architecture 10 Tips to be followed in selecting an architecture 2 PPT with LCD TB1	6	Atomic and Critical Section	2+2	BB	TB1	
architecture of 8051 microcontroller and programming model, registers 3+2 Image: Second State S	7		1+1	BB	TB1	
Image: Non-State of the selecting an architecture Image: Non-State of the selecting an architecture 10 Different AL programs of 8051 2 BB TB2 10 Different AL programs of 8051 2 BB TB2 Actual date of completion: Remarks: UNIT-2 9 Round Robin architecture P Round Robin With Interrupts Architecture Function-queue Scheduling 2+1 BB TB1 I0 Tips to be followed in selecting an architecture 2 PPT with LCD TB1	8	architecture of 8051 microcontroller	3+2	BB	TB2	
Actual date of completion: Remarks: UNIT-2 9 Round Robin architecture Round Robin With Interrupts Architecture Function-queue Scheduling Architecture Real-Time Operating systems Architecture 10 Tips to be followed in selecting an architecture 2 PPT with LCD	9	Instruction set of 8051	1	BB	TB2	
Remarks: UNIT-2 9 Round Robin architecture BB TB1 9 Round Robin With Interrupts 2+1 BB TB1 9 Function-queue Scheduling 2+1 Image: Scheduling and architecture Image: Scheduling and architecture 10 Tips to be followed in selecting an architecture 2 PPT with LCD TB1	10	Different AL programs of 8051	2	BB	TB2	
9 Round Robin architecture BB TB1 Round Robin With Interrupts Architecture 2+1 BB TB1 Function-queue Scheduling Architecture 2+1 Image: Comparison of the second		rks:				
Round Robin With Interrupts Architecture2+12+1Function-queue Scheduling Architecture2+1Real-Time Operating systems Architecture210Tips to be followed in selecting an architecture22PPT with LCDTB1		UNIT-2				
architecture ² LCD	9	Round Robin With Interrupts Architecture Function-queue Scheduling Architecture Real-Time Operating systems	2+1	BB	TB1	
Actual date of completion:	10	~ -	2		TB1	
	Actua	l date of completion:				

Rema	rks:				
	UNIT-3				
11	Tasks and Task States Tasks and Data	2	BB	TB1	
15	Semaphores and Shared Data	5+3	PPT with LCD	TB1	
16	Message Queues, Mail boxes and Pipes	3+2	BB	TB1	
17	Timer Functions	1	BB	TB1	
18	Events	2	PPT with LCD	TB1	
Rema	rks: UNIT-4				
19	RTOS Overview Principles	2+1	BB	TB1	
Actua Rema					
	UNIT-5	Γ			1
26	Host and Target Machines Cross Compilers	3+2	BB	TB1	
27	Linker/Locators for Embedded Software	2	BB	TB1	
28	Getting Embedded software into the target system	3+2	PPT with LCD	TB1	

29	Testing on your Host Machine		BB	TB1		
	Instruction Set Simulators,	3+1				
	Logic Analyzers, In-circuit Emulators,Monitors					
Actual	date of completion:	I	I	I	I	
Remar	ks:					
	UNIT-6					
30	IOT introduction	2	BB	TB3		
31	IOT communication	1	BB	TB3		
Actual	date of completion:	I				
Remar	ks:					
	Total classes	95				
Actual	Actual syllabus completion:					
Faculty	Faculty Remarks:					
HoD R	HoD Remarks:					