PULSE & DIGITAL CIRCUITS

LABORATORY MANUAL

R16

III / IV B.E (ECE)

I - SEMESTER

DEPT. OF ELECTRONICS & COMMUNICATION ENGINEERING

SIR C.R.REDDY COLLEGE OF ENGINEERING
ELURU-534007

VISION AND MISSION OF THE COLLEGE

Vision:

To ignite the minds of the students through academic excellence so as to bring about social transformation and prosperity.

Mission:

1. To provide valued added research and development.
2. To embody a spirit of excellence in teaching, creativity, scholarship and outreach.
3. To provide a platform for synergy of academy, industry and community.
4. To inculcate high standards of ethical and professional behavior.

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VISION AND MISSION OF THE DEPARTMENT

Vision:

In pursuit of world class excellence in the field of Electronics& Communication Engineering by imparting quality education and promoting Research.

Mission:

1. To empower students with knowledge and competencies in the field of Electronics& Communication Engineering conforming to International standards.
2. To produce creative solutions essential to local and global needs in the field of Electronics& Communication Engineering.
3. To mould the students professionally with a consciousness of moral values and professional ethical code.

COURSE STRUCTURE

SUBJECT	T	P/D	C
Computer Architecture and Organization	3+1*	-	3
Linear IC Applications	3+1*	-	3
Digital IC Applications	3+1*	-	3
Digital Communications	3+1*	-	3
Antennas and Wave Propagation	3+1*	-	3
Pulse and Digital circuits Lab	-	3	2
LIC Applications Lab	-	3	2
Digital IC Applications Lab	-	3	2
Professional Ethics and Human Values	3		--
Total	**23**	**9**	**21**

PULSE & DIGITAL CIRCUITS
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III / IV B.E (ECE)

I - SEMESTER

LIST OF EXPERIMENTS

1. Linear wave shaping.
2. Non Linear wave shaping – Clippers.
3. Non Linear wave shaping – Clampers.
4. Transistor as a switch.
5. Study of Logic Gates & Some applications.
6. Study of Flip-Flops & some applications.
7. Sampling Gates.
8. Astable Multivibrator.
9. Monostable Multivibrator.
10. Bistable Multivibrator.
11. Schmitt Trigger.
12. UJT Relaxation Oscillator.
13. Bootstrap sweep circuit.

EQUIPMENT REQUIRED FOR LABORATORY:

1. RPS - 0 – 30 V
2. CRO - 0 – 20 M Hz.
3. Function Generators - 0 – 1 M Hz
4. Components
5. Multi Meters

1. LINEAR WAVE SHAPING

Aim:

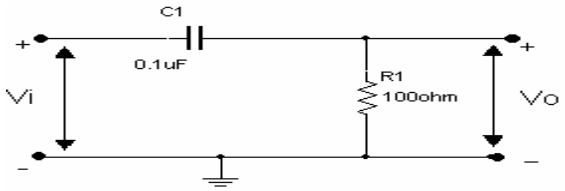
Design a RC LPF and HPF at various time constants and verify the responses for Square wave input (choose C = 0.1μf, V_i =V= 4 VP-P, f = 10 K Hz).

Apparatus:

S.No	Name of the component/Equipments	Specification	Quantity
1.	Resistors	10KΩ	1
2.	Capacitors	10 μf 1 nf 100 nf	1 1 1
3.	Bread board		1
4.	Connecting wires		1 Bunch
5.	Function generator		1
6.	CRO		1
7.	Decade resistance box		1

Circuit diagram:

HIGH PASS FILTER:



Theory:

The output of HP RC network is the differentiation of the applied input signal. Hence this type of network is called differentiator. It was seen that for a high pass RC network,

$d/dt(Vi)=d/dt(Vo)+V_0/RC$

$=> d/dt(Vo)=d/dt(Vi) - 1/RC$

If the time constant =RC is far less than the periodic time (RC/T<<1), the transient response becomes insignificant and the steady state response becomes predominant,

Ignoring the transient response, $(1/RC)\ V_0 = d/dt(vi)$

(or) $V_0 = RC\ d/dt(vi)$

Since R and C are of fixed magnitude

$V_0 \alpha\ d/dt(vi)$

i.e; the output is proportional to the time derivative of the input. Hence the circuit is called as differentiator

Design / Calculations:

RC = T

Given T = 1/10 KHz = 0.1 mSec

R= (0.1 X10 $^{-3}$) /0.1μf = 1 K ohms.

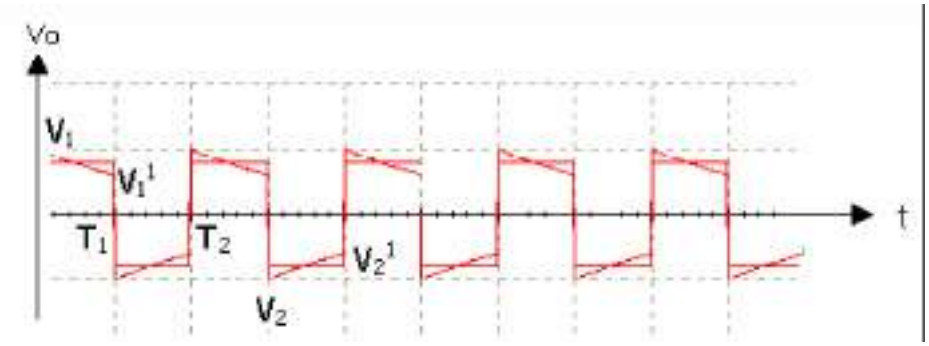
V_1= V / (1+ e $^{-T/2RC}$) =2.49v

V_1'' = $\frac{V}{1+e^{T/2RC}}$

=1.51 V

% tilt =2 (V^1-$V^{1''}$)/V = (2.49-1.51)/2 = 49%

Model Graph:



T1=T2=T/2

b) RC >> T

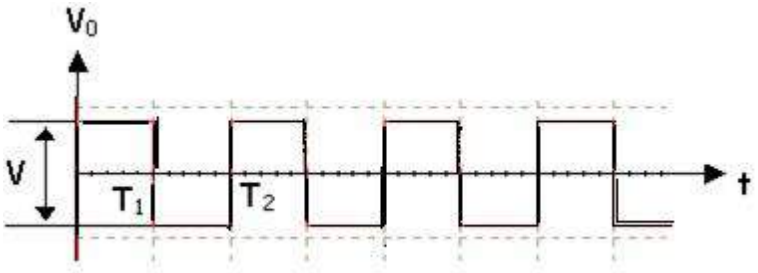
Choose RC = 10T = 1 m Sec

R= (10 $^{-3}$)/ (0.1x10 $^{-6}$)

=10 k ohms

The output waveform will be identical to input

Model Graph:



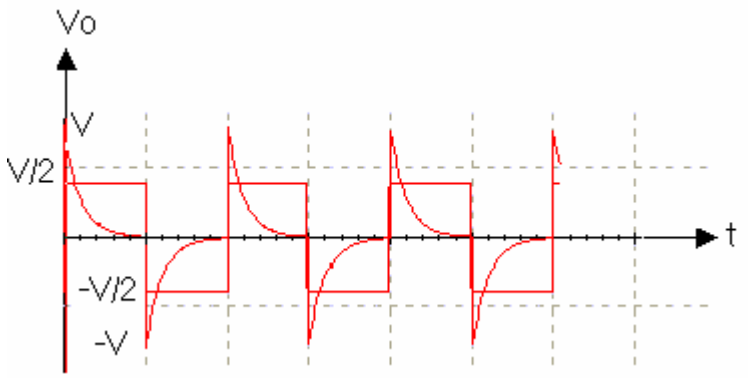
T1=T2=T/2

RC << T

RC = 0.1 T

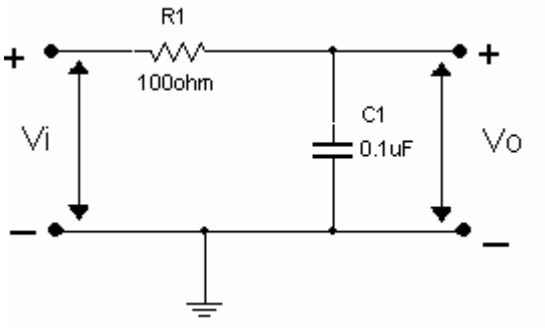
R= (0.1x 10 $^{-4}$)/(0.1x10 $^{-6}$)

Model Graph:



LOW PASS FILTER:

Circuit Diagram:



Theory:

We know that for a low pass RC circuit V0/RC +d/dt(V_0) =Vi/RC Where RC is the time constant of the circuit. Let it be assumed that RC >>T, the periodic time of the input signal V_i.

For a large time constant, it is evident that the output takes a fairly long time to come to steady state and as such the transient response is very predominant and the steady state response becomes insignificant and hence can be ignored.

Put, (1/RC) V_0=0, we

have d/dt(Vo) =(1/RC)Vi

By integrating on both sides, we get

$V_0 = (1/RC) \int Vi\, dt.$

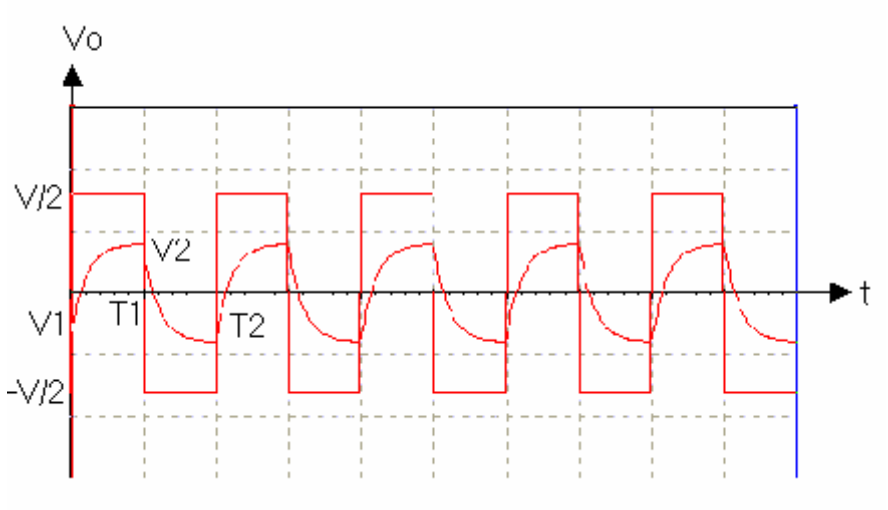
$V_0 \alpha \int Vi\, dt$ i.e; R,C are fixed magnitude .

And the output is proportional to the time integral of the input. For this reason the low pass RC circuit with RC>>T is called integrator.

Design / Calculations:

(a) RC=T
C=0.1µf , R= 1K Ohms
V2=V(e $^{T/2RC}$ -1) /2 (e $^{T/2RC}$ +1) =0.49V
V1=-0.49v

Model Graph:

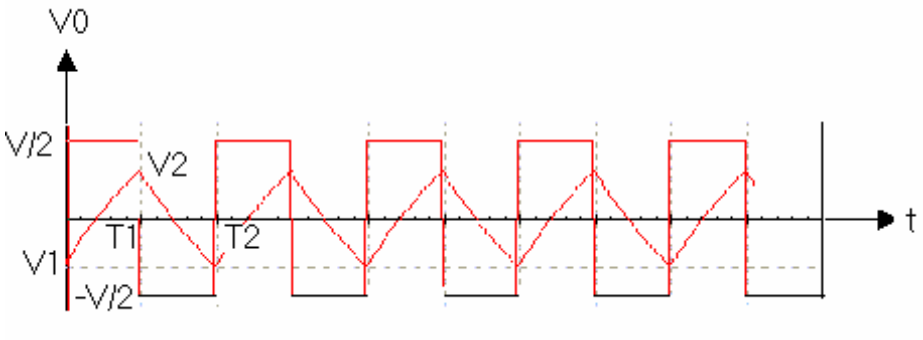


(b) RC >> T
R = 10 KΩ, C = 0.1 µf

V2=V (e $^{T/2RC}$ -1) /2 (e $^{T/2RC}$ +1) =0.05V

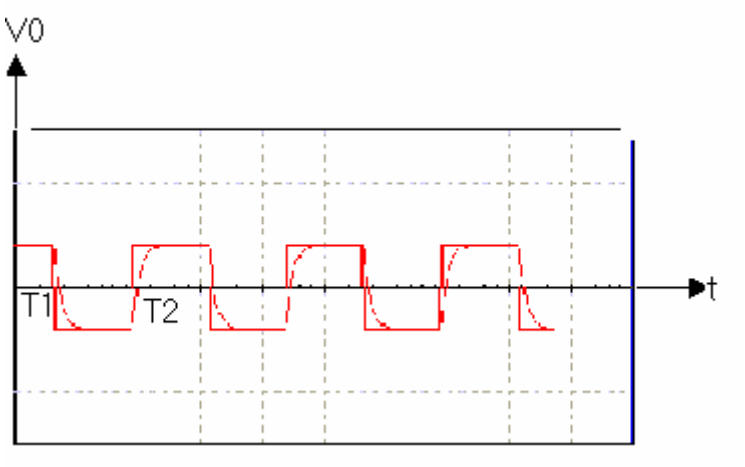
V1=0.05V

Model Graph:



(c) RC << T
R = 100Ω,
C = 0.1 µf

Model Graph:



Note:

Low Pass Filter allows the DC component of I/P signal and High Pass Filter block the DC component of I/P Signal.

Procedure:

1. Connect the circuit as shown in figure (LPF / HPF)
2. Apply the Square wave input to this circuit (Vi = 4 VP-P, f = 10KHz)
3. Observe the output waveform for (a) RC = T, (b) RC>>T, (c) RC<<T
4. Verify the values with theoretical calculations.

Precautions:

Use two CRO probes and observe i/p &o/p waveforms simultaneously by putting CRO on DC modes.

Result:

LPF and HPF are designed at various time constants and the responses for square wave input is observed & hence plotted

Questions:

1. When HP-RC circuit is used as Differentiator?
2. Draw the responses of HPF to step, pulse, ramp inputs?
3. Draw the responses of LPF to step, pulse, ramp inputs?
4. Define % tilt and rise time?
5. When LP-RC circuit is used as integrator?
6. Why noise immunity is more in integrator than differentiator?

2. NON-LINEAR WAVE SHAPING CIRCUITS - CLIPPERS

Aim:

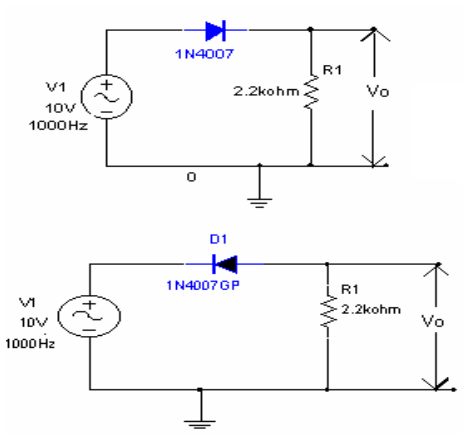
a) To study the clipping circuits using diodes.
b) To observe the transfer characteristics of all the clipping circuits in CRO.

Apparatus:

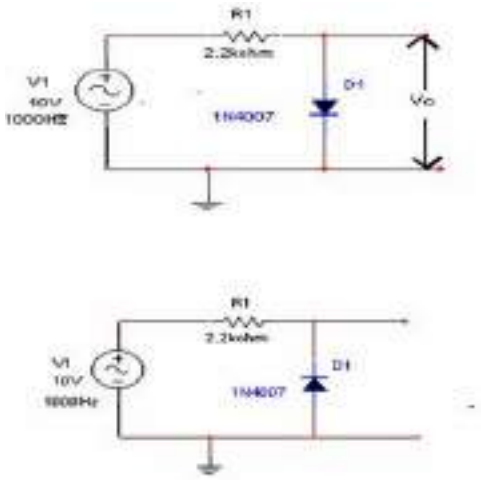
S.No	Name of the component/Equipments	Specification	Quantity
1.	Resistors	1kΩ	1
		10KΩ	1
2.	Diodes	1N4007	1
3.	Bread board		1
4.	Connecting wires		1 Bunch
5.	Function generator		1
6.	CRO		1

Circuit Diagram

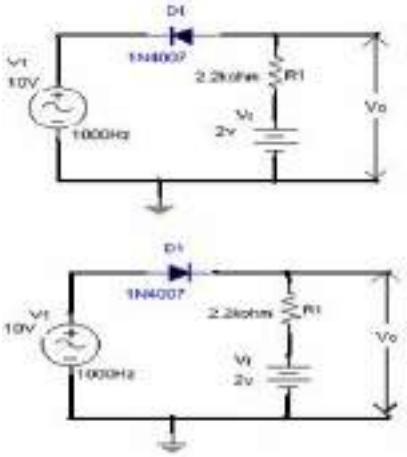
Series Diode Clipper:-



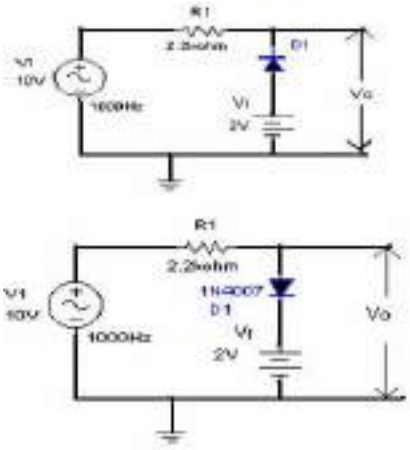
Shunt Diode Clipper:



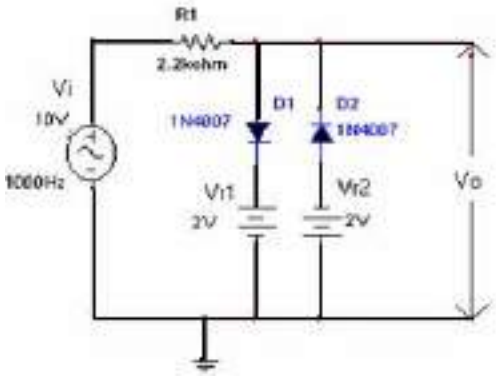
Series Diode Clipper with Bias:



Shunt Diode Clipper with Bias



Slicer:



Theory:

A clipping circuit comprises of linear elements like resistors and non-linear elements like diodes or transistor, but it does not contain energy storage elements capacitors. Clipping circuits basically limit the amplitude of the input signal either below or above certain voltage level. They are referred to as Voltage limiters, Amplitude selectors or Slicers. A clipping circuit is one, in which a small section of input waveform is missing or cut or truncated at the output section. Clipping circuits are classified based on the position of Diode.

1. Series Diode Clipper
2. Shunt Diode Clipper.

Procedure:

1. Connect the circuit as shown in fig.1
2. In each case apply 10 VP-P, 1 KHz Sine wave i/p using a signal generator.
3. O/P is taken across the load RL.
4. Observe the O/P waveform on the CRO and compare with i/p waveform.

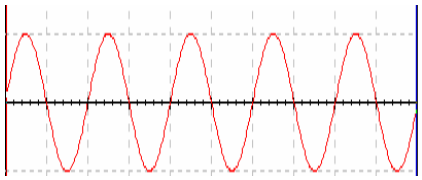
5. Sketch the i/p as well as o/p waveforms and mark the numerical values.
6. Note the changes in the O/P due to variations in the reference voltage
   V_R = 2V, 3V.
7. Obtain the transfer characteristics of Fig.1, by keeping CRO in X-Y mode.
8. Repeat the above steps for all the circuit.

Precautions:

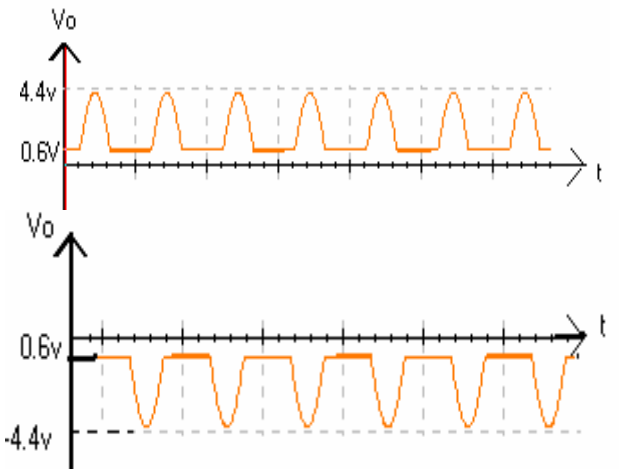
1. Set the CRO O/P channel in DC mode always.
2. Observe the waveform simultaneously by keeping common ground.
3. See that there is no DC component in the I/P.
4. To find transfer characteristics apply input to the X-Channel, O/P to Y-Channel, adjust the dot at the center of the screen when CRO is in X-Y mode. Both the channels must be in ground, then remove ground and plot the transfer characteristics.

Model Graph:

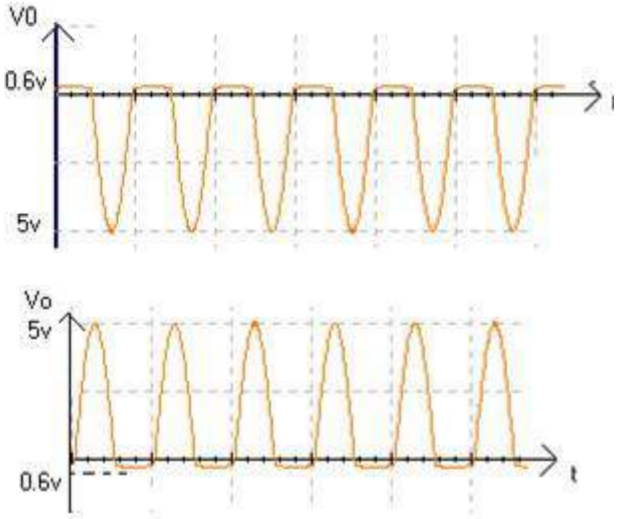
Input Wave Form



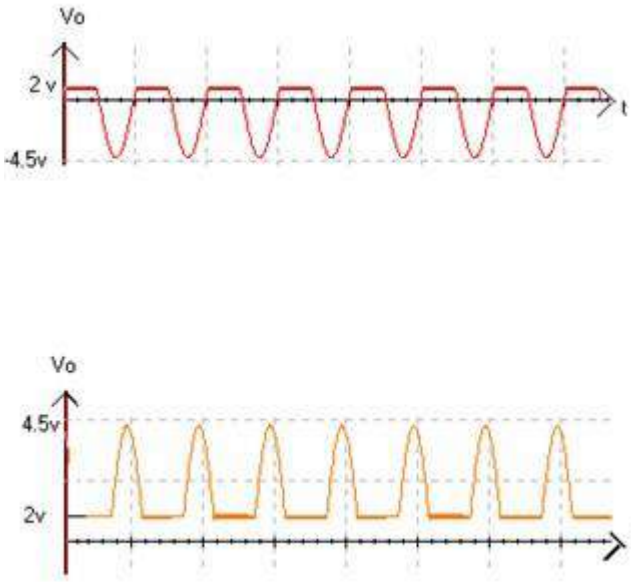
Output wave form for Series Diode Clipper:



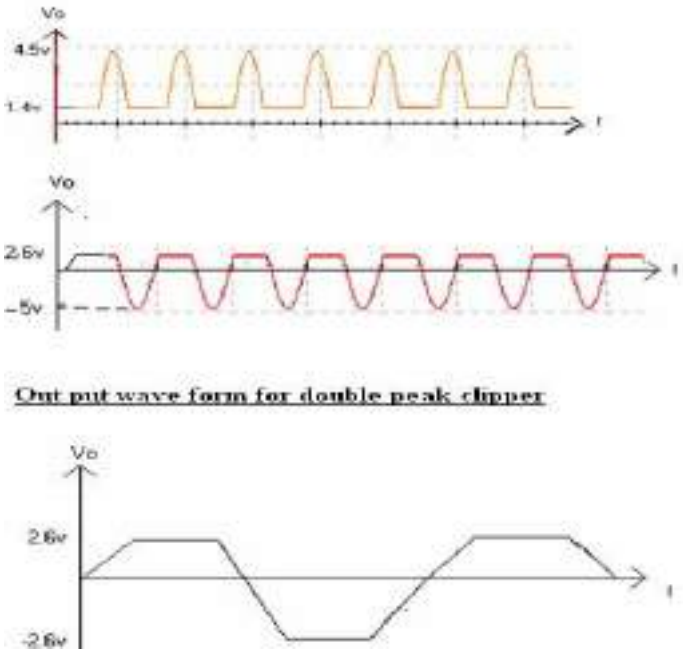
Output wave form for Shunt Diode Clipper:



Output wave form for series Diode Clipper with bias:



Output wave form for shunt Diode Clipper with bias:



Out put wave form for double peak clipper

Result:

Different types of clipping circuits have been studied and observed the responses for various combinations of VR and clipping diodes.

Questions:

1. Define clipping circuit?
2. What are the different types of clippers?
3. What is a break region?
4. Which kind of a clipper is called a slicer circuit?
5. What are the disadvantages of the shunt clipper?
6. What are the disadvantages of the series clipper?
7. What is piecewise linear mode of a diode?

3. NON-LINEAR WAVE SHAPING CIRCUITS - CLAMPERS

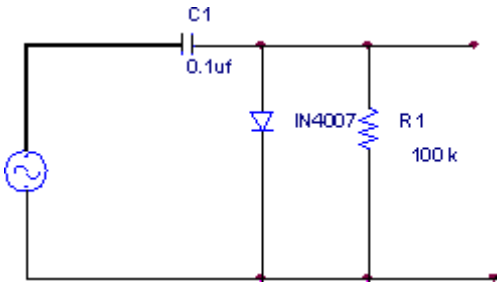
Aim: To study the clamping circuits using diodes and capacitors.

Apparatus:

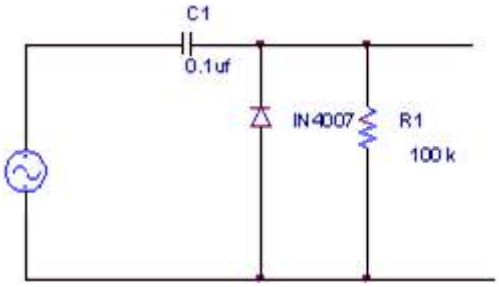
S.No	Name of the component	Specification	Quantity
1.	Resistors	100kΩ	1
2.	Diodes	1N4007	1
3.	Capacitor	0.1µf	
4.	Bread board		1
5.	Connecting wires		1 Bunch
6.	Function generator		1
7.	CRO		1
8.	Dual Regulated Power supply	(0-30) V DC	1

Circuit Diagrams:

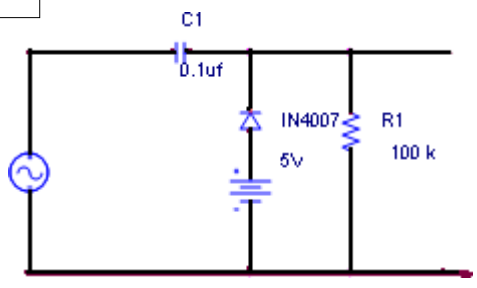
Negative Clamper



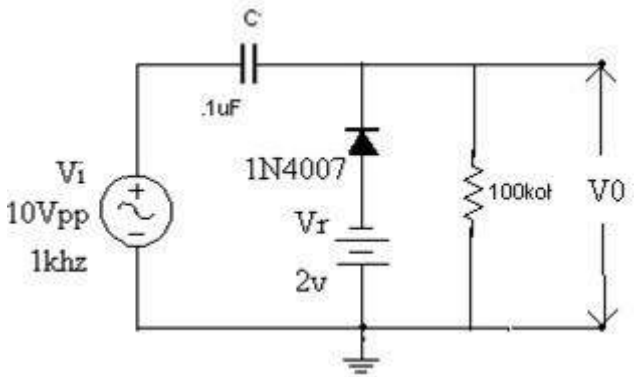
Positive Clamper



Biased –Ve clamper (-Vr)



Biased +Ve Clamper:



Theory:

Clamping circuits add a DC level to an AC signal. A clamper is also refer to as DC restorer or DC reinserted. The Clampers which clamp the given waveform either above or below the reference level, which are known as positive or negative clamping respectively. They are of two types

(i) Negative clamper.

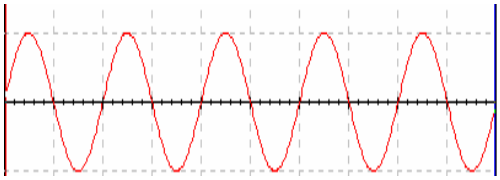
(ii) Positive clamper.

Negative clamper is also termed as positive peak clamper, since circuit clamps the positive peak to zero level. Similarly positive clamper is termed as negative peak clamper, since the circuit clamps the negative peak to zero level.

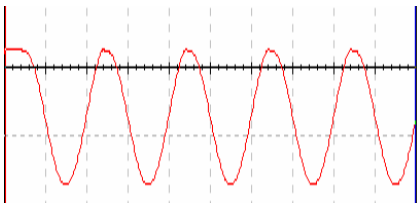
Procedure:

1. Connect the circuit as shown in fig.1.
2. Apply a Sine wave of 10VP-P, 1KHz at the input terminals with the help of Signal Generator.
3. Observe the I/P & O/P waveforms of CRO and plot the waveforms and mark the values with VR =2 V, 3V
4. O/P is taken across the load RL.
5. Repeat the above steps for all clamping circuits as shown.
6. Waveforms are drawn assuming diode is ideal.

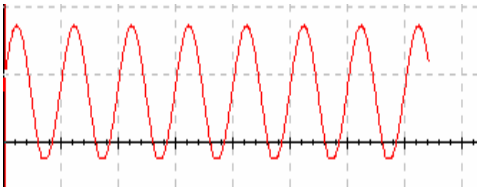
Model graph: I/P Wave Form



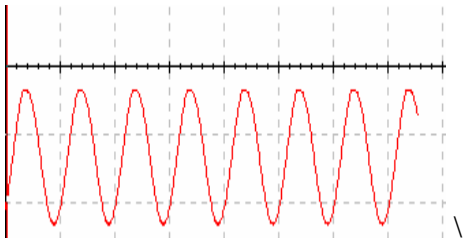
Out put wave forms for –ve Clamper:



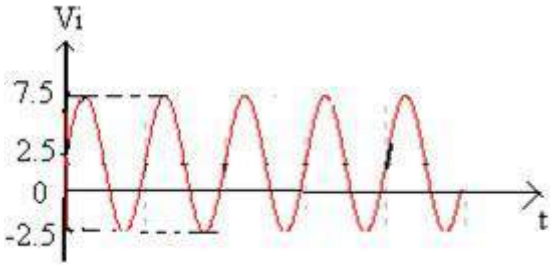
Out put wave forms for +ve Clamper:



Biased –Ve Clamper



Biased +Ve Clamper:



Result:

Different types of clamping circuits are studied and observed the response for different combinations of V_R and diodes.

Questions: 1.What are the applications of clamping circuits?

2. What is the synchronized clamping?

3. Why clamper is called a dc inserter?

4. TRANSISTOR AS A SWITCH

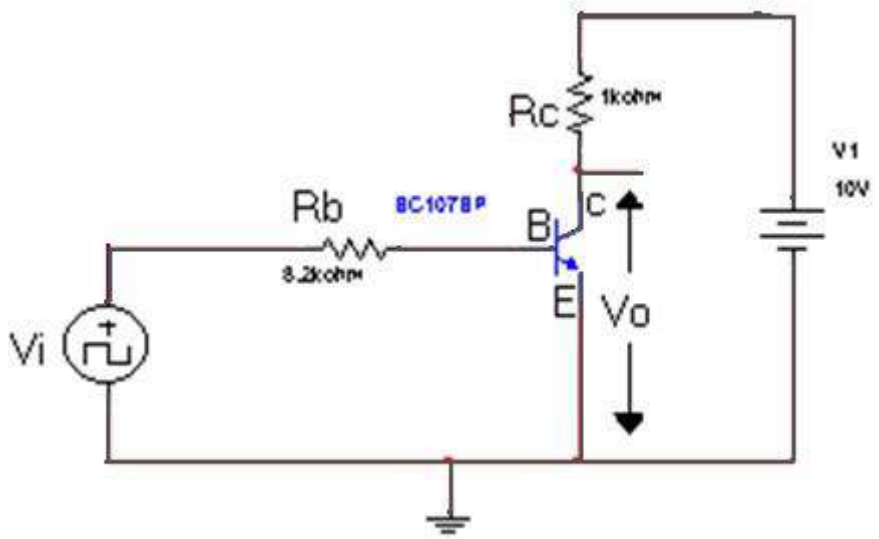
Aim:

Design Transistor act as a Switch and verify the operation. Choose V_{CC} = 10V, $I_{C\,max}$ = 10 m A, h_{fe} =50, $V_{CE\,Sat}$ = 0.2, V_{in} = 4Vp-p, $V_{BE\,Sat}$ = 0.6 V.

Apparatus:

S.No	Name of the component	Specification	Quantity
1.	Resistors	1kΩ	1
		8.2kΩ	1
2.	Transistor	BC 107	1
3.	Bread board		1
4.	Connecting wires		1 Bunch
5.	Function generator		1
6.	CRO		1
7.	Dual Regulated Power supply	(0-30) V DC	1

Circuit Diagram:



Theory:

When the I/P voltage V_i is negative or zero, transistor is cut-off and no current flows through Rc , henceV_0= V_{CC} when i/p Voltage V_i jumps to positive voltage, transistor will be driven into saturation. Then

$V_0 = Vcc - I_C R_C = V_{CEsat}$

Design procedure:

When Q is ON Then

$Rc = (Vcc - V_{CE\ sat}) / Ic\ max$

$= (10-0.2)/10\ mA$

$= 1\ k\ ohms$

$I_B \geq I_C\ max / hfe$

$\geq 10mA / 50$

$I_B \geq 0.2\ mA$

To keep transistor remains ON, I_B should be greater than

$V_{in} = I_B R_B + V_{BE\ Sat}$

$2V = 0.2\ mA\ R_B + 0.6V$

$R_B = 7\ K\ ohms$ (choose practical values as 8.2 K Ω)

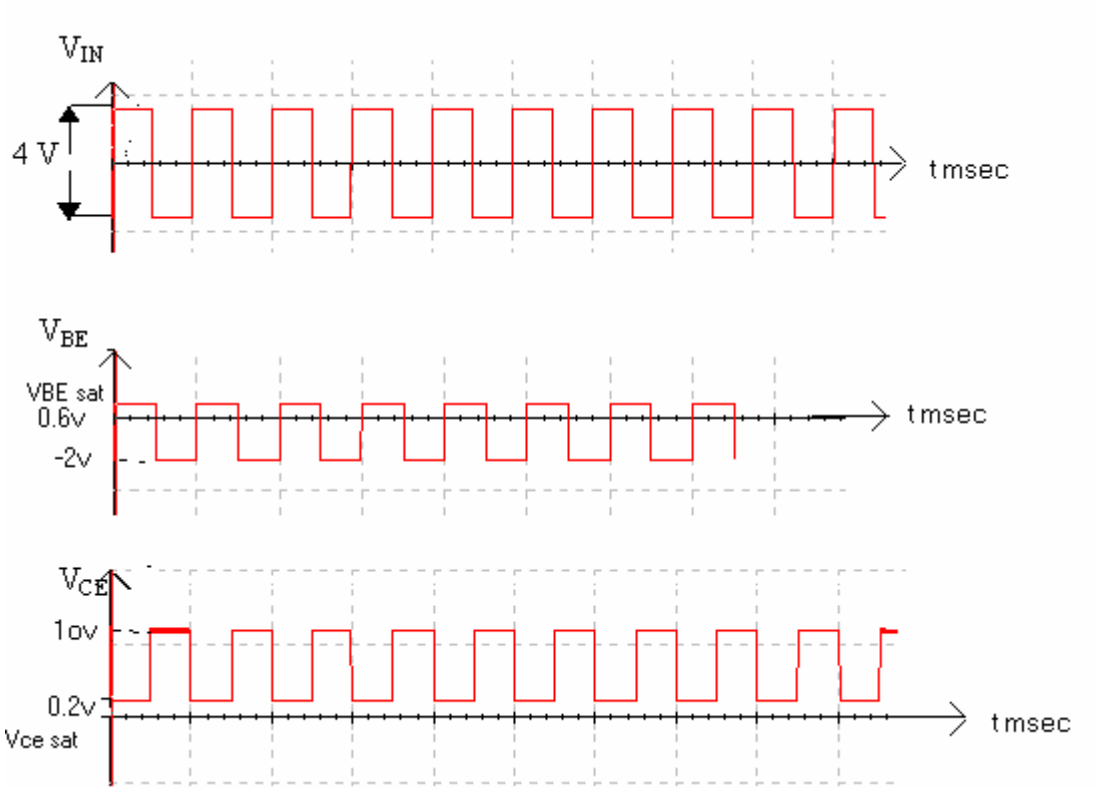
Procedure:-

1. Connect the circuit as shown in figure.
2. Apply the Square wave 4 Vp-p frequency of 1 KHz
3. Observe the waveforms at Collector and Base and plot it.

Precautions: -

1. When you are measuring O/P waveform at collector and base, keep the CRO in DC mode.
2. When you are measuring VBE Sat, VCE Sat keep volts/div switch at either 0.2 or 0.5 position.
3. When you are applying the square wave see that there is no DC voltage in that. This can be checked by CRO in either AC or DC mode, there should not be any jumps/distortion in waveform on the screen.

Model Graph:



Result:

Transistor as a switch has been designed and O/P waveforms are observed. .

Questions:

1. Differentiate between Diode and Transistor as a switch?
2. Mention typical values of VBE Sat, VCE Sat for both Si, Ge Transistors?
3. Define ON time, OFF time of the transistor?
4. In which regions Transistor acts as a switch?
5. Explain phenomenon of "latching "in a Transistor switch?
6. Define Rise time & fall time of a transistor switch?

5. Study of Logic gates and Applications

Aim:

To verify the truth table of logic gates USING DISCRETE COMPONENTS and also Verify the truth table

Apparatus:

S.No	Name of the component	Specification	Quantity
1.	Resistors	1kΩ	1
		8.2kΩ	1
2.	Transistor	BC 107	1
3.	Bread board		1
4.	Connecting wires		1 Bunch
5.	Function generator		1
6.	CRO		1
7.	Dual Regulated Power supply	(0-30) V DC	1

Theory:

NOT, AND, OR gates are called as basic gates & NAND, NOR gates are called as Universal gates we can implement the basic logic gates using the universal gates.

i) NOT gate: - The NOT gate is also called as an inverter, since it performs the inversion operation on the given input. For instance if the input is logic 1, the output is the compliment of it i.e. logic 0. And if the input is logic 0 then the output is logic 1 vice versa.

ii) AND gate: - The output of this gate is 1 if and only if both the inputs are high i.e. logic 1, otherwise logic 0.

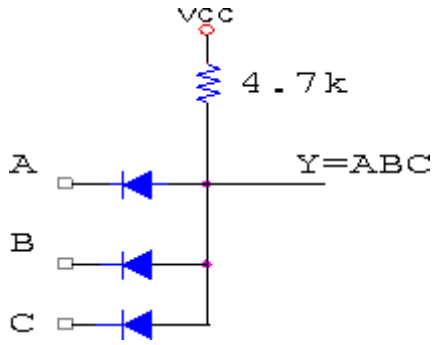
iii) OR gate:- The output of this gate is low only when both the inputs are low, otherwise logic 1

iv) NAND gate: This gate is compliment to the AND gate .The output of this gate is LOW only when both the inputs are high, otherwise 1

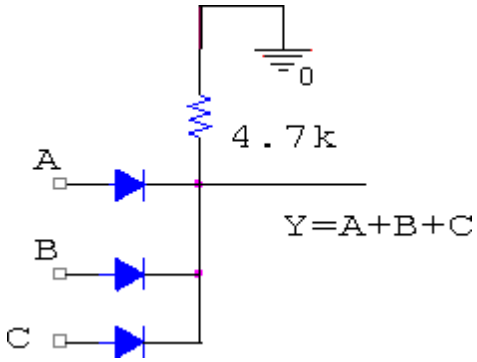
v) NOR gate: - This gate is the compliment of the OR gate. The output of this gate is high only when both the inputs are low otherwise 0

vi) EX-OR gate:- The output of this gate is 1 only when the no. of inputs are odd otherwise 0

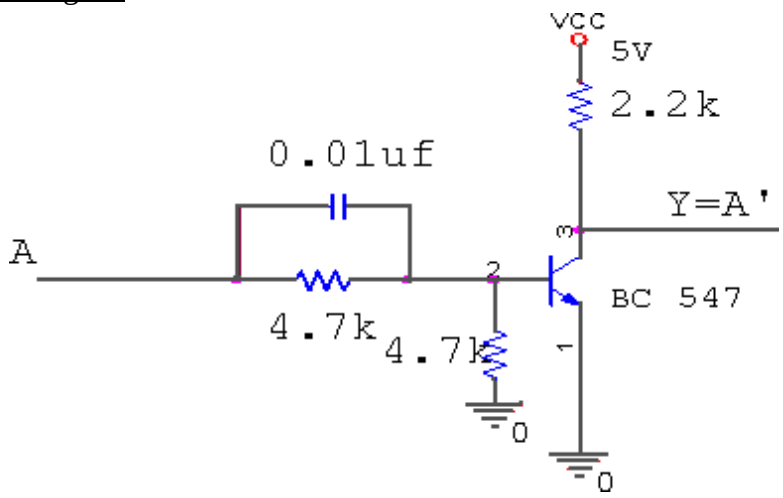
AND gate



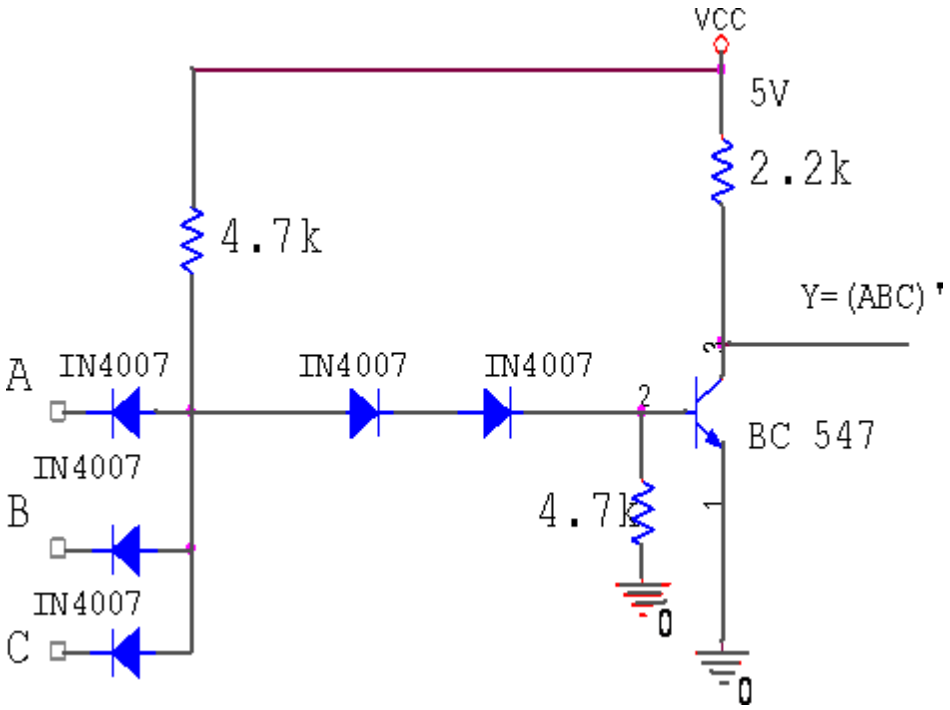
OR gate:



NOT gate:



NAND gate:



Procedure:-

1. Connect the logic gates on the breadboard as per the circuit diagram
2. Apply 5V to one terminal and 0V to another terminal of AND gate and note down the output voltage same way take input voltages as (0V, 5V), (0V, 0V) & (5V, 5V) and note the output voltages.
3. Similarly repeat this procedure for all the logic gates and universal gates like NAND & NOR and note down the o/p voltages in each case.

Result:

The truth tables of all the logic gates (NOT, AND, OR), Universal gates (NAND, NOR) and Half adder, Full adder circuits are also verified successfully.

Questions:

1. Why NAND & NOR gates are called universal gates?
2. Realize the EX – OR gates using minimum number of NAND gates.
3. Give the truth table for EX-NOR (EX-OR+NOT) and realize using NAND gates.
4. Realize the given logic expression using NAND and also using NOR gates.F = A‟BC+A‟B„C+AB„C„
5. Explain the operation of NAND gate when realized using discrete components.
6. In which regions the transistor is operated like a Switch.
7. What are the logic low and High levels of TTL IC„s and CMOS IC„s.
8. Compare TTL logic family with CMOS family.
9. Which logic family is called fastest and which logic family is called low power dissipated.
10. Explain the operation of OR, NOR gates when realized using discrete Components
11. Why the transistor operates as NOT gate.

6. STUDY OF FLIP FLOPS

AIM: To study and verify the characteristic table of RS, D, JK, and T Flip flops.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Flip Flop trainer kit		1
2.	Connecting wires		

THEORY:

A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

RS FLIP FLOP:
The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form. The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

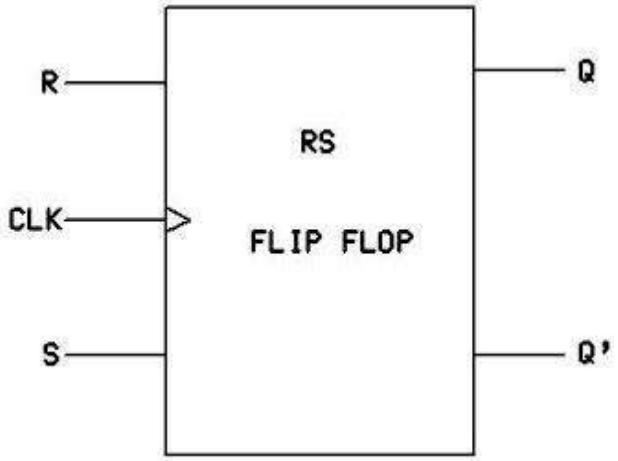
D FLIP FLOP:
To eliminate the undesirable condition of indeterminate state in the SR Flip Flop when both inputs are high at the same time, in the D Flip Flop the inputs are never made equal at the same time. This is obtained by making the two inputs complement of each other.

JK FLIP FLOP:
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q‟ is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q‟ output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

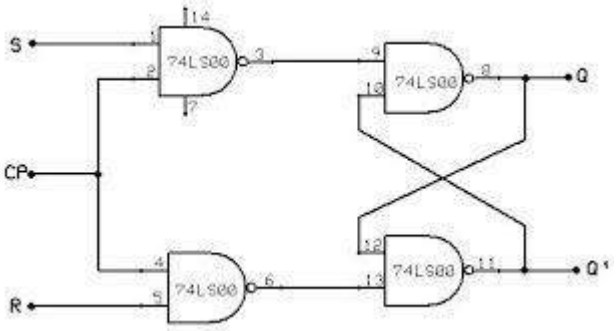
T FLIP FLOP:
This is a modification of JK Flip Flop, obtained by connecting both inputs J and K inputs together. T Flip Flop is also called Toggle Flip Flop.

RS FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

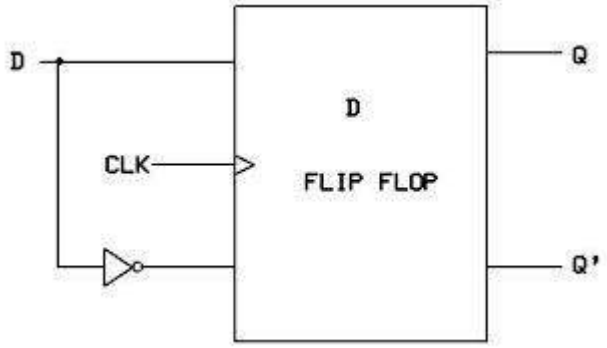


CHARACTERISTIC TABLE:

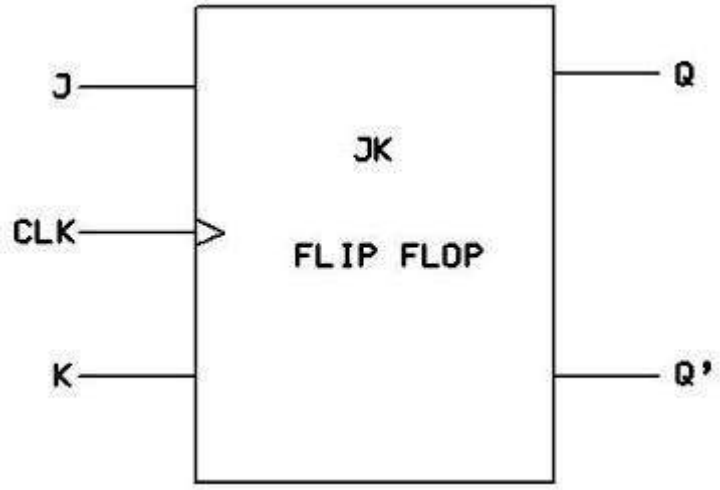
CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	S	R			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	X	
8	1	1	1	X	

D FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

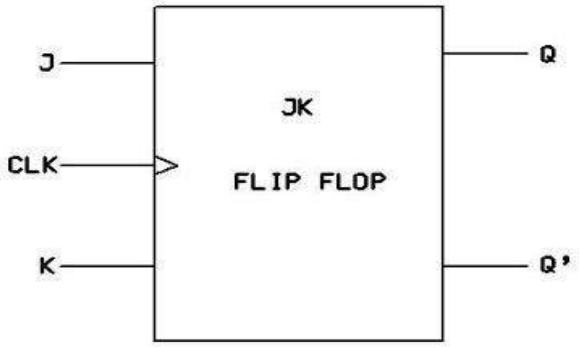


CHARACTERISTIC TABLE:

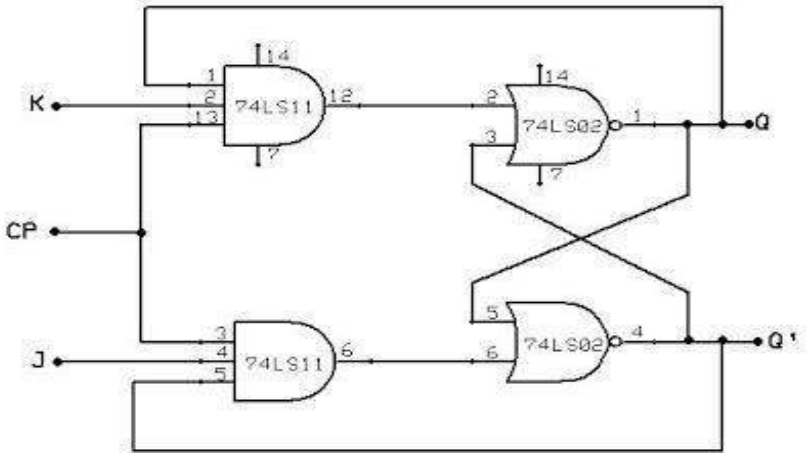
CLOCK PULSE	INPUT D	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	1	

JK FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

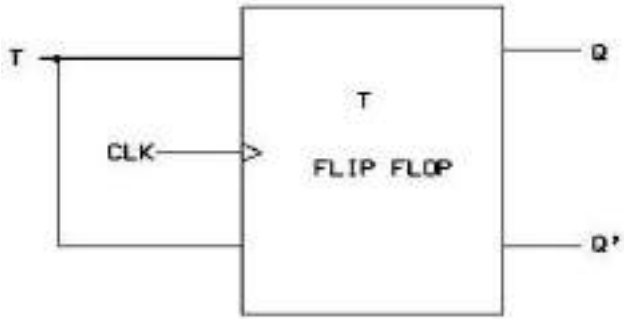


CHARACTERISTIC TABLE:

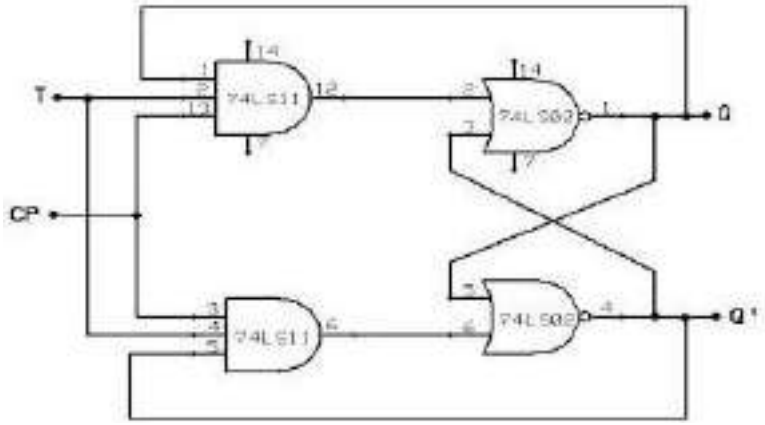
CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	J	K			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	0	

T FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT T	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	0	

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and observe the status of all the flip flops.

RESULT:
The Characteristic tables of RS, D, JK, T flip flops were verified.

7. SAMPLING GATES

Aim:

To study the output wave form of the Uni-directional diode sampling gate

Apparatus:

s.no	Name of the component	Specification	Quantity
2.	Resistors	10kΩ 1kΩ	2 1
3.	Diode	IN4007	2
4.	Capacitors	0.1uf	1
5.	RPS		1
6.	Bread board		1
7.	Connecting wires		-----
8.	Function generator		1
9.	CRO		1

Theory:

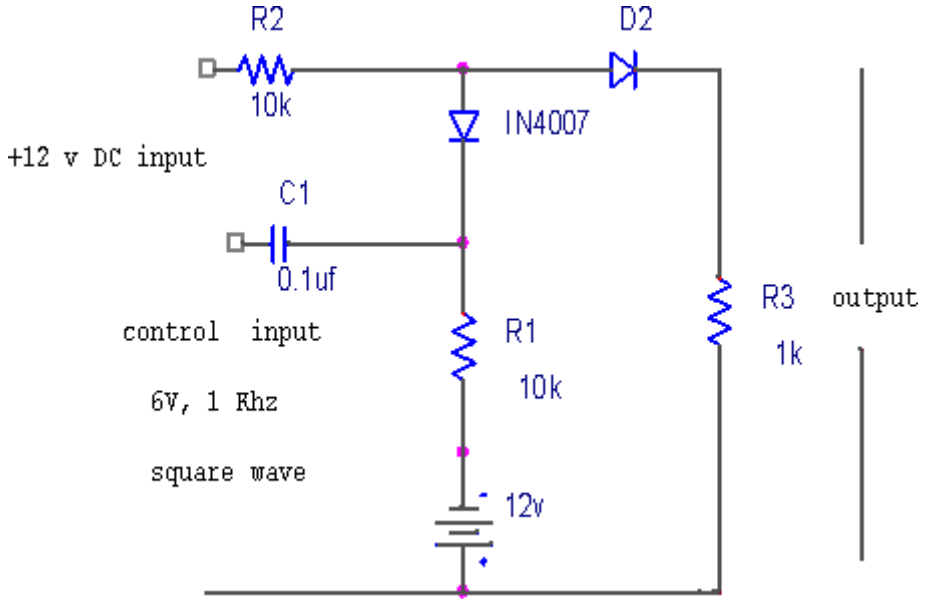
In the absence of the control signal, it is easily seen that diode D_1 is forward biased and hence it conducts. The current through R develops a large voltage drop across it with the result that the voltage at A is less than the cut-in voltage of D_0. Hence there is no conduction through D_0, and the output is zero.

If a positive going control signal is applied, it is evident that diode D_1 gets reverse biased and hence conduction through it stops. Diode D_0 gets forward biased and as a result the input signal gets transmitted through the gate for the duration of control signal.

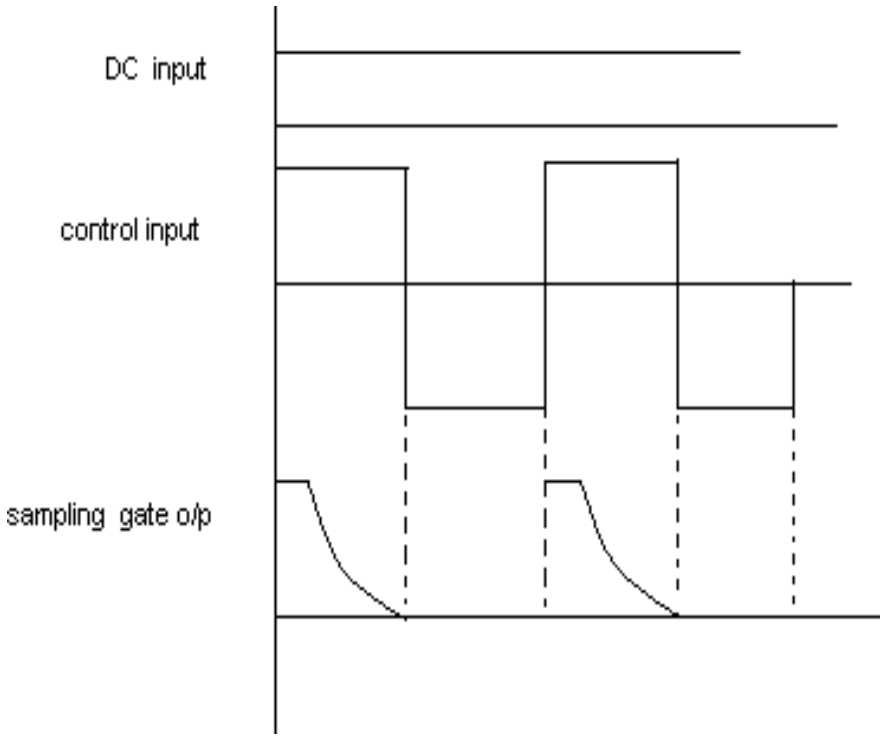
Procedure:

1. Connect the circuit as per the circuit diagram on bread board
2. Apply input 12V dc supply and control signal is 6V square wave
3. Take the output across the R_L and note the amplitude and time period
4. Tabulate the readings and draw the graph

Circuit diagram:



Expected wave forms:



Result: Thus the output wave form of sampling gate is observed

8. ASTABLE MULTIVIBRATOR

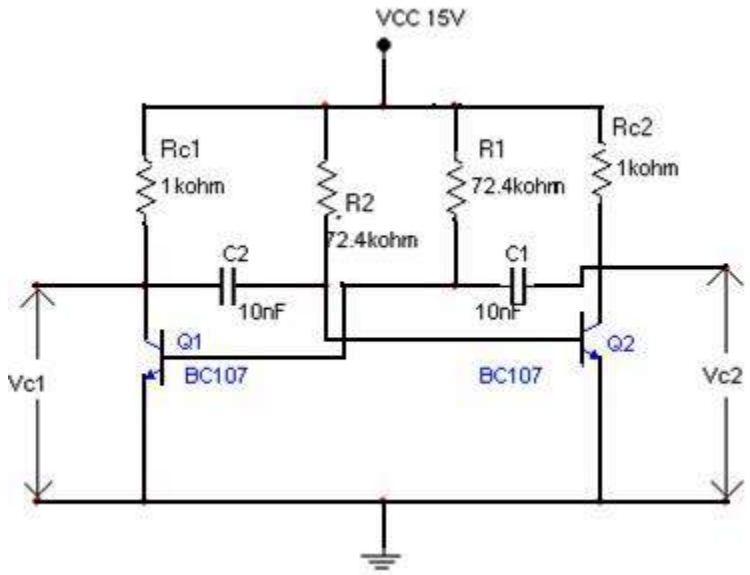
Aim :-

To design an Astable Multivibrator to generate a Square wave of 1KHzfrequency. Choose C = 1nf, 10nf, 100nf.

Apparatus:

S.No	Name of the component	Specification	Quantity
1.	Resistors	1kΩ	2
		72kΩ	2
		724kΩ	2
		7.2kΩ	2
2.	Transistor	BC 107	2
3.	Bread board		1
4.	Connecting wires		1 Bunch
5.	CRO		1
6.	Dual Regulated Power supply	(0-30) V DC	1

Circuit diagram:-



Theory:

The astable circuit has two quasi-stable states. Without external triggering signal the astable configuration will make successive transitions from one quasi-stable state to the other. The astable circuit is an oscillator. It is also called as free running multivibrator and is used to generate "Square Wave". Since it does not require triggering signal, fast switching is possible.

Design:

The period T is given by

$T = T1 + T2 = 0.69 (R1C1 + R2C2)$

For symmetrical circuit with R1 = R2 = R & C1 = C2 = C

$T = 1.38 RC$

$10^{-3} = 1.38 \times 10^{-9} \times R$

$R = 72.4K\Omega$ (When c=1nf) ;

$R= (10^{-3}) /1.38X10X10^{-9}$

$=72.4 K \Omega$ (where c=10nf)

$R=7.24 K \Omega$ (where =100nf)

Let Vcc=15V, h_{fe}=51(for BC 107)

Vbe sat=0.7V, Vce sat=0.3 V

Choose Ic max=10 mA

$RC = (V_{CC} – V_{CESat}) / I_{Cmax}$

$= (15 – 0.3) / (10 \times 10\text{-}3) = 1.47K\Omega$

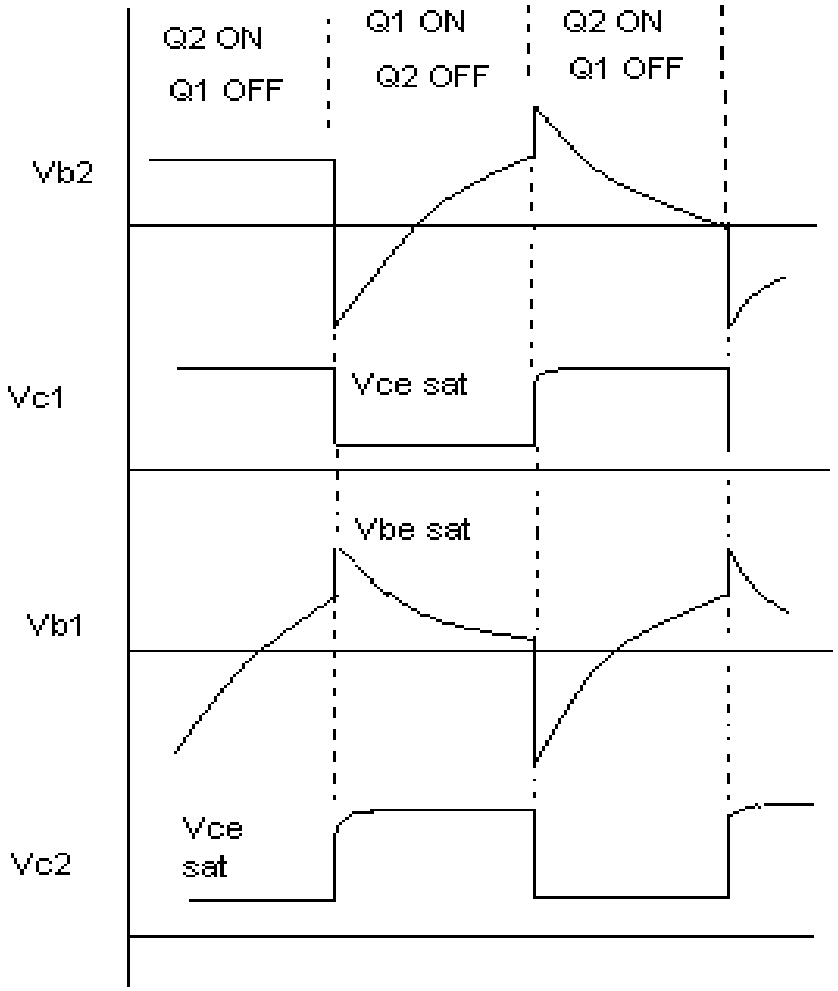
$\therefore$ RC =1KΩ

Procedure:

1. Connect the circuit as shown in figure.
2. Apply the supply voltage Vcc =15V
3. Calculate the pulse width (T) of the Astable O/P with the selected values of R & C on the CRO. See that CRO is in DC mode.
4. Connect the CRO channel-1 to the collector and base of the Transistor Q_1&$Q_{2..}$
5. Measure the pulse width and verify with the theoretical value.
6. Obtain waveforms at different points like V_{B1}, V_{B2}, V_{C1} & V_{C2}.

.

Expected wave forms:-



Result : An Astable Multivibrator is designed, the waveforms are observed and verified the results theoretically.

Questions:

1. Is it possible to change time period of the waveform without changing R & C? Support your answer?
2. Collector waveforms are observed with rounded edges. Explain?
3. Explain charging and discharging of capacitors in an Astable Multivibrator?
4. How can an Astable multivibrator be used as VCO?
5. Why do you get overshoots in the Base waveforms?
6. What are the applications of Astable Multivibrator?

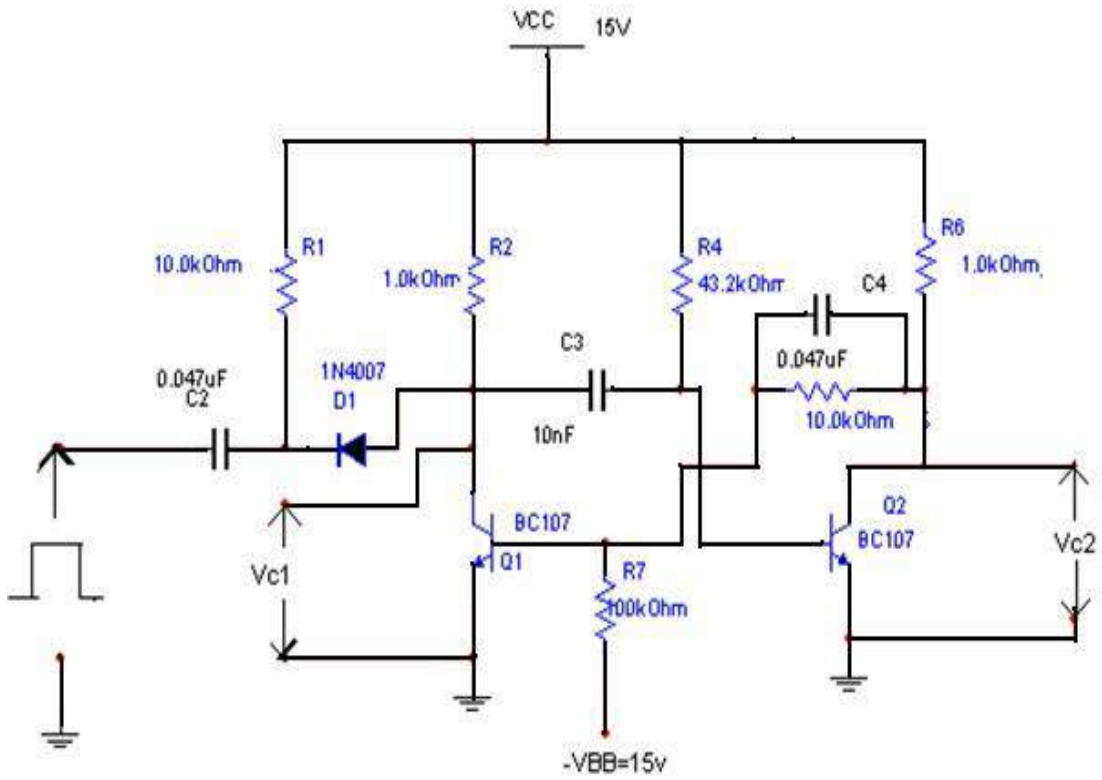
9.MONOSTABLE MULTIVIBRATOR

Aim : To design a monostable multivibrator for the Pulse width of 0.03mSec.

Apparatus:

S.No	Name of the component	Specification	Quantity
1.	Resistors	1kΩ	2
		72kΩ	2
		724kΩ	2
		7.2kΩ	2
2.	Transistor	BC 107	2
3.	Bread board		1
4.	Connecting wires		1 Bunch
5.	CRO		1
6.	Dual Regulated Power supply	(0-30) V DC	1

Circuit Diagram:-



Theory:

The monostable circuit has one permanently stable and one quasi-stable state. In the monostable configuration, a triggering signal is required to induce a transition from the stable state to the quasi-stable state. The circuit remains in its quasi-stable for a time equal to RC time constant of the circuit. It returns from the quasi-stable state to its stable state without any external triggering pulse. It is also called as one-shot a single cycle, a single step circuit or a univibrator

Design:-

To design a monostable multivibrator for the Pulse width of 0.03mSec.

Choose ICmax = 15mA, VCC = 15V, VBB = 15V, R1 = 10KΩ.

$T = RC \ln 2$

$T = 0.69\ RC$

Choose C = 10nf

$0.3 \times 10^{-3}\text{Sec} = 0.69 \times R \times 10 \times 10^{-9}$

R = 43.47 KΩ.

Rc= (Vcc- Vce sat)/ Ic max.

RC = (15 – 0.2) / 15mA = 1kΩ

For more margin Given,

VB1= -1.185

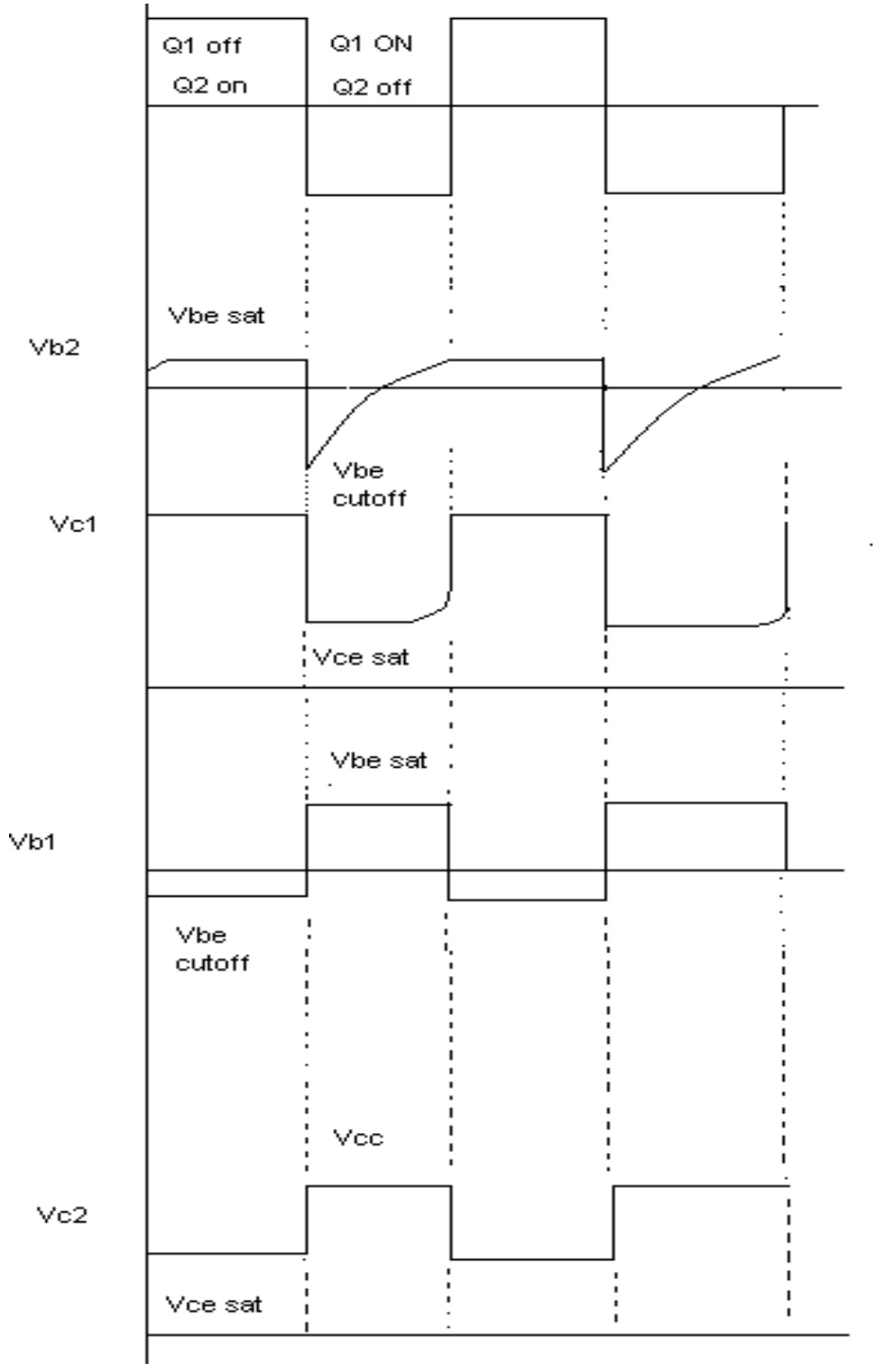
$$VB1 = \frac{-V_{BB} R_1}{R1+R2} + \frac{Vce\ sat\ R_2}{R1+R2}$$

-1.18 = (-15 R1+ 0.2 R2) / (R1+R2)

Given R1=10 KΩ

We will R2= 100K

Expected wave forms:



Procedure:

1. Wire the circuit as shown in the circuit diagram.
2. Calculate the pulse width (T) of the Monostable O/P with the selected values of R & C on the CRO. See that CRO is in DC mode.
3. Select the triggering pulse such that the frequency is less than 1/TApply the triggering input to the circuit and to the CRO‟s channel 1 .
4. Connect the CRO channei-2 to the collector and base of the TransisterQ1&Q2..
5. Adjust the triggering pulse frequency to get stable pulse on the CRO and now measure the pulse width and verify with the theoretical value.
6. Obtain waveforms at different points like VB1, VB2, V_{C1} & V_{C2}.
7. Repeat the experiment for different combinations of R & C (C = 1nf, 100nf). Calculate R for same value of T = 0.3 mSec.

Result :

A collector coupled Monostable Multivinbrator is designed, the waveforms are Observed and verified the results theoretically.

10. BISTABLE MULTIVIBRATOR

Aim:

a) Design the Bi-stable Multivibrator circuit and verify the operation.

b) Obtain the resolving time of Bi-stable Multivibrator and verify theoretically Choose R_1 = 10KΩ, C = 0.3μf, $V_{ce(sat)}$ = 0.2V, IC_{max} = 15mA, V_{CC} = 15V, V_{BB} = 15V, V_{B1} = -1.2V

Apparatus:

s.no	Name of the component	Specification	Quantity
1.	Transistor	BC107b	2
2.	Diode	IN4007	3
3.	Resistors	1kΩ 10kΩ 100kΩ	5 2 2
4.	Capacitors	0.33uf 0.001uf	3 2
5.	RPS		1
6.	Bread board		1
7.	Connecting wires		---
8.	CRO		1

Theory:

A Bistable circuit is one which can exist indefinitely in either of two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. The Bistable circuit is also called as Bistable multivibrator, Eccles jordon circuit, Trigger circuit, Scale-of-2 toggle circuit, Flip-Flop & Binary.

A bistable multivibratior is used in a many digital operations such as counting and the storing of binary information. It is also used in the generation and processing of pulse-type waveform. They can be used to control digital circuits and as frequency dividers.

There are two outputs available which are complements of one another. i.e. when one output is high the other is low and vice versa .

Design:

$R_c = [V_{cc} – V_{ce\,(sat)}] / I_{c(max)}$

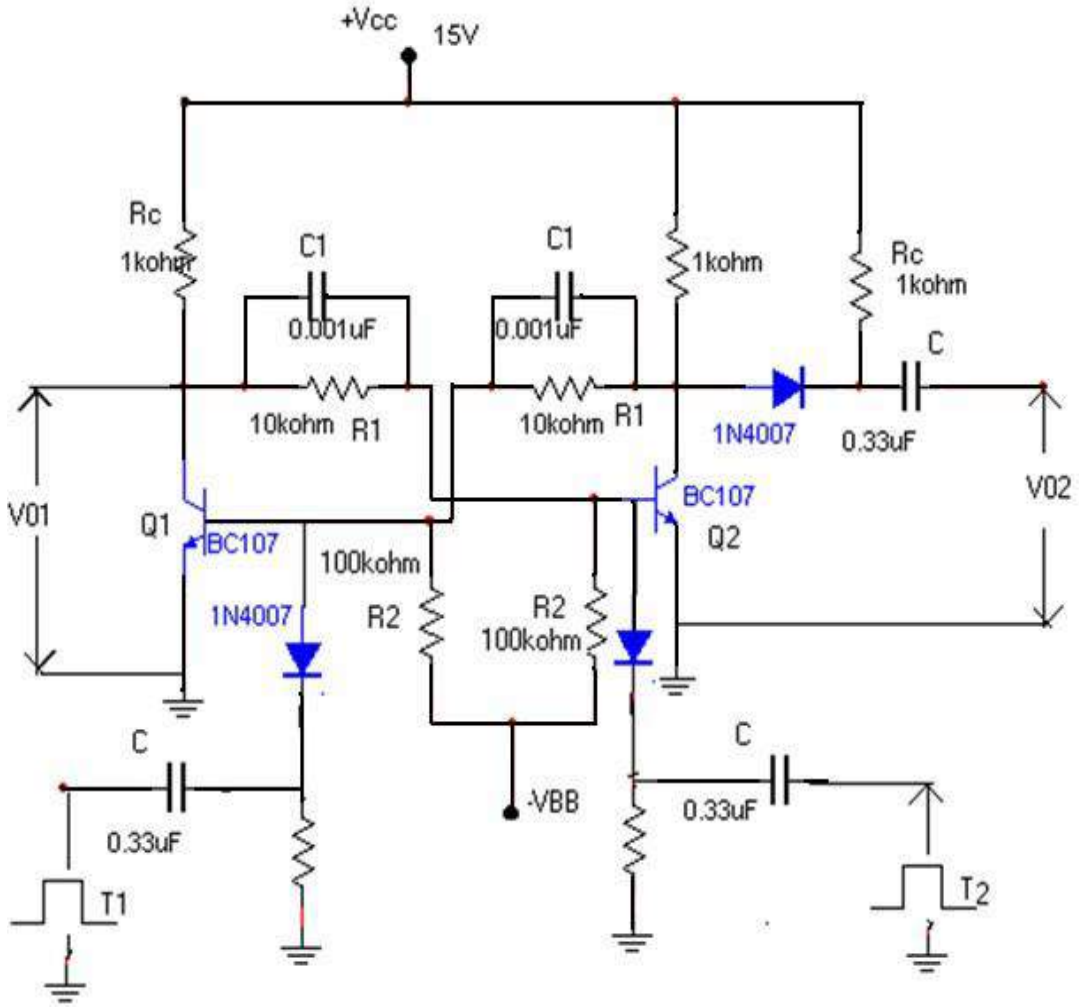
$RC = (15 – 0.2) / 15mA \approx 1K\Omega$

Choose $RC = 1K\Omega$, $VB1 = (-V_{bb}\, R_1 / R_1 + R_2) / (V_{ce\,(sat)}\, R_2 / R_1 + R_2)$

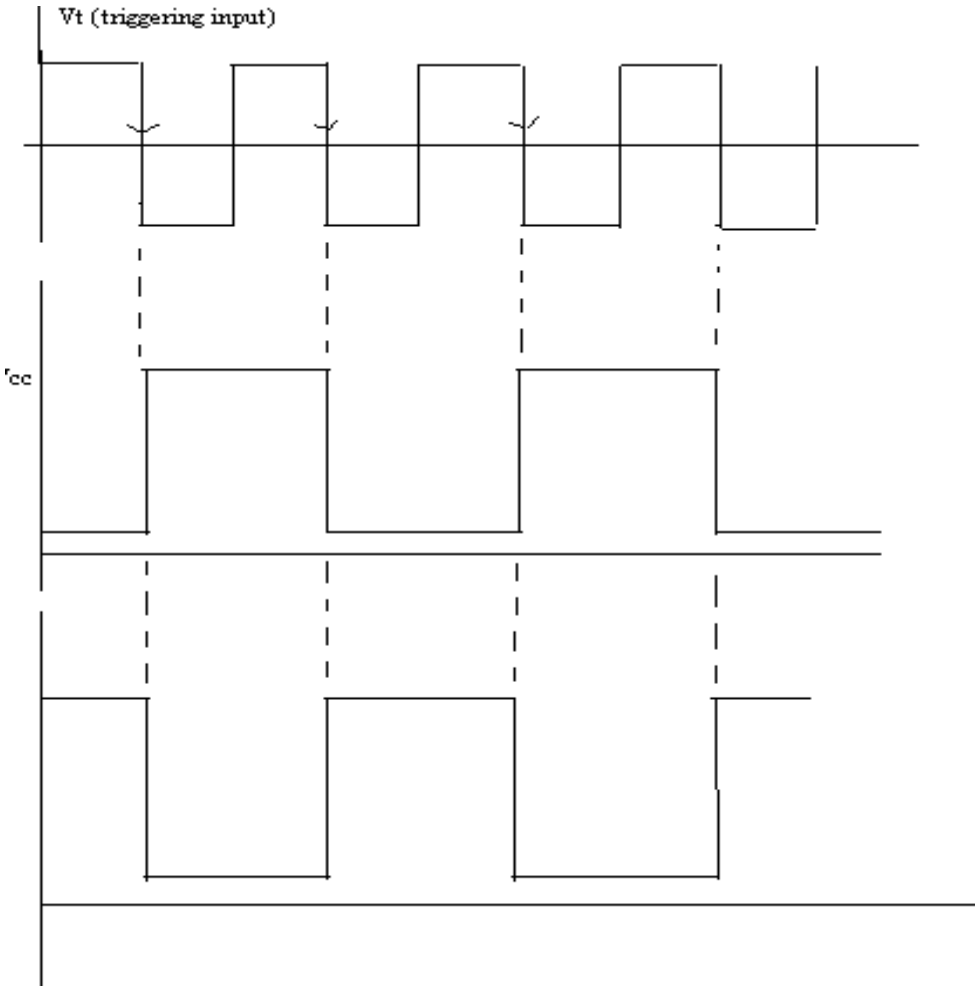
$-1.2 = (-15x10+0.2R_2)/(10+ R_2)$; $R_2 = 100k\Omega$

$f_{max} = (R_1+R_2)/2CR_1R_2$
$= (10+100k)/(2x0.3x10^{-6}x10kx100k)$
$= 55$ kHz

Circuit diagram:



Expected waveforms:



Procedure:

1. Check the square wave output from CRO to conform the voltage is $0.5V_{pp}$.
2. Connect the circuit as shown in the circuit diagram
3. Apply sine wave as input at the transistor Q_1 across collector and emitter terminals
4. Check whether the output waveform at the transistor Q_2 is square wave or not
5. Measure the amplitude of output wave form and check whether the loop gain is less than 1
6. Similarly apply the input at transistor Q_2
7. Repeat the steps 3 and 4 and note down the amplitude and output waveform

Result:

Bistable Multivibrator circuit is designed and output waveforms are observed

11. SCHMITT TRIGGER

Aim:-

To study the operation of Schmitt trigger circuit and find the UTP and LTP voltages & compare with the theoretical values.

Apparatus:

s.no	Name of the component	Specification	Quantity
1.	Transistor	BC107a	2
2.	Resistors	1kΩ 10kΩ 100kΩ	2 2 2
4.	Capacitors	0.1uf	1
5.	RPS		1
6.	Bread board		1
7.	Connecting wires		-----
8.	Function generator		1
9.	CRO		1

Theory:

Schmitt trigger is a special type of bistable multivibrator which has several important practical applications. The Schmitt trigger is a emitter coupled binary. Since the emitter of Q_1 and Q_2 are joined and they are grounded through a common resistor R_e. The base of Q_1 is connected to a voltage source V_i. The output is an unsymmetrical square wave. Thus the Schmitt trigger converts the sinusoidal wave to square. It is therefore termed as sine to square wave converter or squaring circuit.

However the output of a Schmitt trigger is a square wave, whatever the waveforms of the input signal. Another application of Schmitt trigger is as a flip-flop.

Theoretical calculations:

i) Calculation of V_1 [UTP]

$V_1 = V^1 - 0.1V$ where $V^1 = (V_{cc}\ R_2)/(RC_1+R_1+R_2)$

$V^1 = (V_{cc}\ R_2)/(RC_1+R_1+R_2)$

=>12x10k / (1k+10k+10k) = 5.714V

$V_1 = UTP = V^1 - 0.1V$

= 5.714V – 0.1V

= 5.61V

ii) Calculation of V_2 [LTP]

$a = R_2/(R_1+ R_2)$

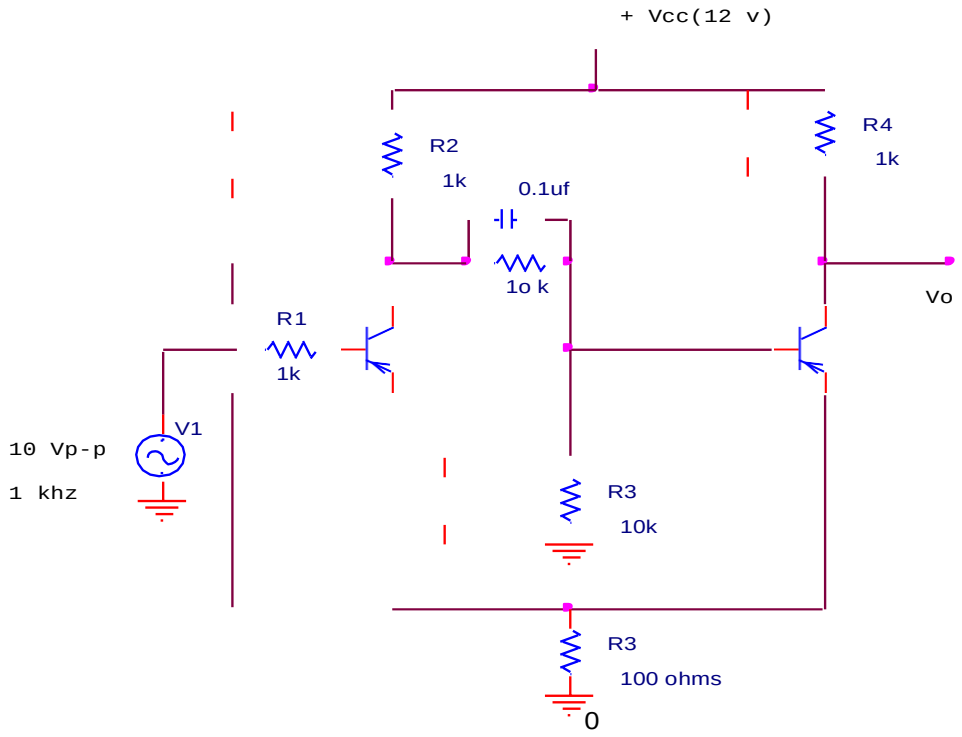
= 10k/(10k+10k) =0.5

$V^1 = aV_T$

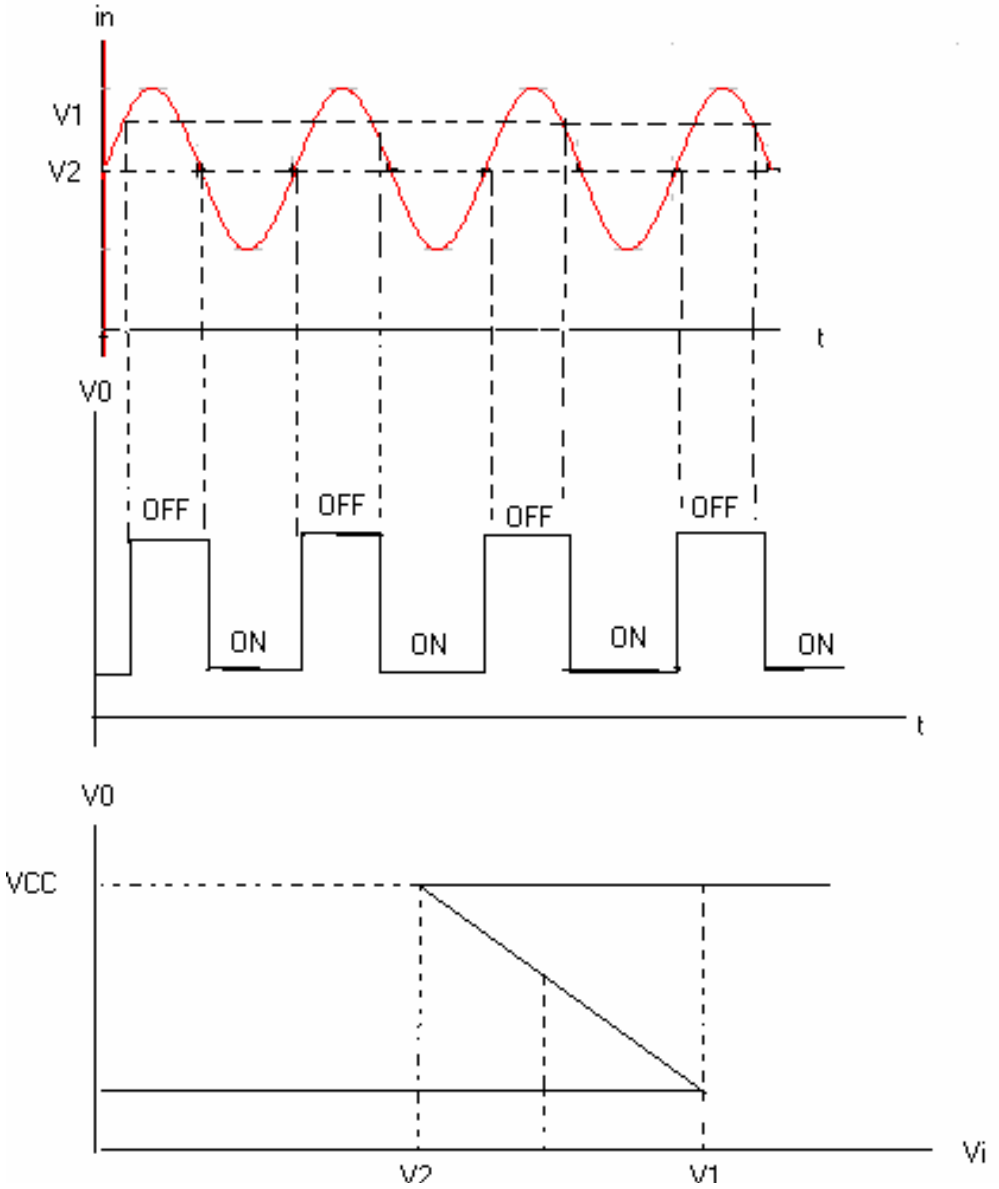
=> 0.5x12V =6V (since $V_T = V_{cc}$)

$R = RC_1 (R_1 + R_2)/ (RC_1+R_1+R_2)$
$= 1k (10k+10k)/ (1k+10k+10k)$
$= 952.38\Omega$
$V_{BE1} = 0.6V$ & $V_{\gamma 2} = 0.6V$
$V_2 = V_{BE1} + (R_e/aR + R_e) (V1 - V_{\gamma 2})$
$= 0.6 + [100/ (0.5 \times 952.38) + 100] (6-0.6)$
$= 1.53V$

Circuit diagram :



Expected wave form



Procedure:

1. Connect the circuit on the bread board as per circuit diagram
2. Keep the peak to peak input voltage 10V using function generator
3. Keep the V_{CC} voltage at 12V constant using regulated power supply
4. Observe the output waveform in the CRO
5. Plot the values and draw the graph
6. Calculate the upper triggering point & lower triggering point

Result:

The operation of Schmitt trigger is verified and the UTP & LTP voltages in both theoretically and practically compared and verified

12. UJT RELAXATION OSCILLATOR

Aim:

To study the operation of UJT Relaxation Oscillator

Apparatus:

s.no	Name of the component	Specification	Quantity
1.	UJT	2N2646	1
2.	Resistors	68Ω 560Ω 100kΩ	1 1 1
4.	Capacitors	0.1uf	1
5.	RPS		1
6.	Bread board		1
7.	Connecting wires		-----
8.	Function generator		1
9.	CRO		1

Theory:

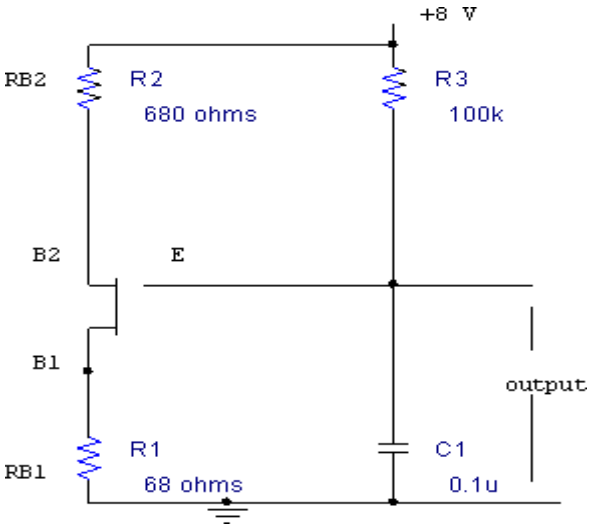
The UJT exhibits a negative resistance characteristics, it can be used to provide time delayed trigger pulses for activating other devices like SCR. The basic trigger circuit is shown in the figure.

The external resistances R_{B1} and R_{B2} are of the UJT base. The emitter potential V_e is varied depending on the charging rate of capacitor C. The Charging resistance Rc should be such that the load line intersects the device characteristics only, in the negative resistance region AB. If the Rc load line intersects the device characteristics either in region PR or in BQ ,the resulting operating point will be stable and the circuit will not oscillate. This sets the max and minimum limits on the permissible values of Rc.

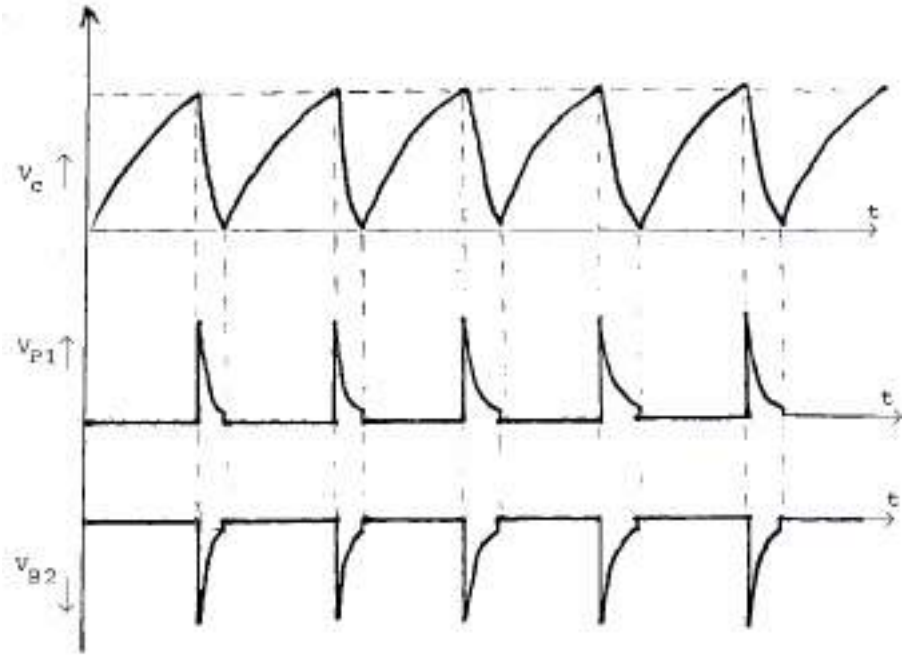
As the Capacitor charges, when the emitter voltage goes to the peak point voltage (ηV_b+V_D) , regeneration will start and the capacitor will discharges through resistor R_{B1}. The rise time of the output pulse will depend on the switching speed of the UJT, and the duration will be proportional to the time constant $R_{B1}C$ of the discharge circuit. The emitter – base -1 diode will again be reverse biased until the capacitor is charged to (ηV_b+V_D) . The output pulses are shown in figure and the duration and their period T is given by

$$T = RC \ln (1/1-\eta)$$

Circuit diagram:



Expected waveforms:



Procedure:

1. Connect the circuit on the bread board as per circuit diagram
2. A resistor of 68Ω is connected to B_1 and 560Ω resistor is connected to B_2
3. Apply V_{CC}= 8V to the resistor 100kΩ and B_2
4. Take the output across the emitter of UJT
5. Note down the time period and amplitudes of output waveform

Result:

The waveforms are plotted as shown and the practical T is verified to the theoretical value.

13. BOOTSTRAP SWEEP GENERATOR

Aim:

To study the operation of a Boot strap sweep generator

Apparatus:

s.no	Name of the component	Specification	Quantity
1.	Transistor	CL100S	1
2.	Resistors	10Ω 1kΩ 470Ω	1 1 1
3.	Diode	IN4148	1
4.	Capacitors	0.1uf 100uf	1 2
5.	RPS		1
6.	Bread board		1
7.	Connecting wires		-----
8.	Function generator		1
9.	CRO		1
10.	Decade resistance box		1

Theory:

The circuit employs positive feed back and it generates positive going ramp and employs an emitter follower whose gain is nearly unity. The amplifier must have high input resistance. In this the capacitor current can be maintained constant by incorporating an auxiliary voltage source such that the source voltage is always equal to the capacitor voltage but acts in opposition to it.

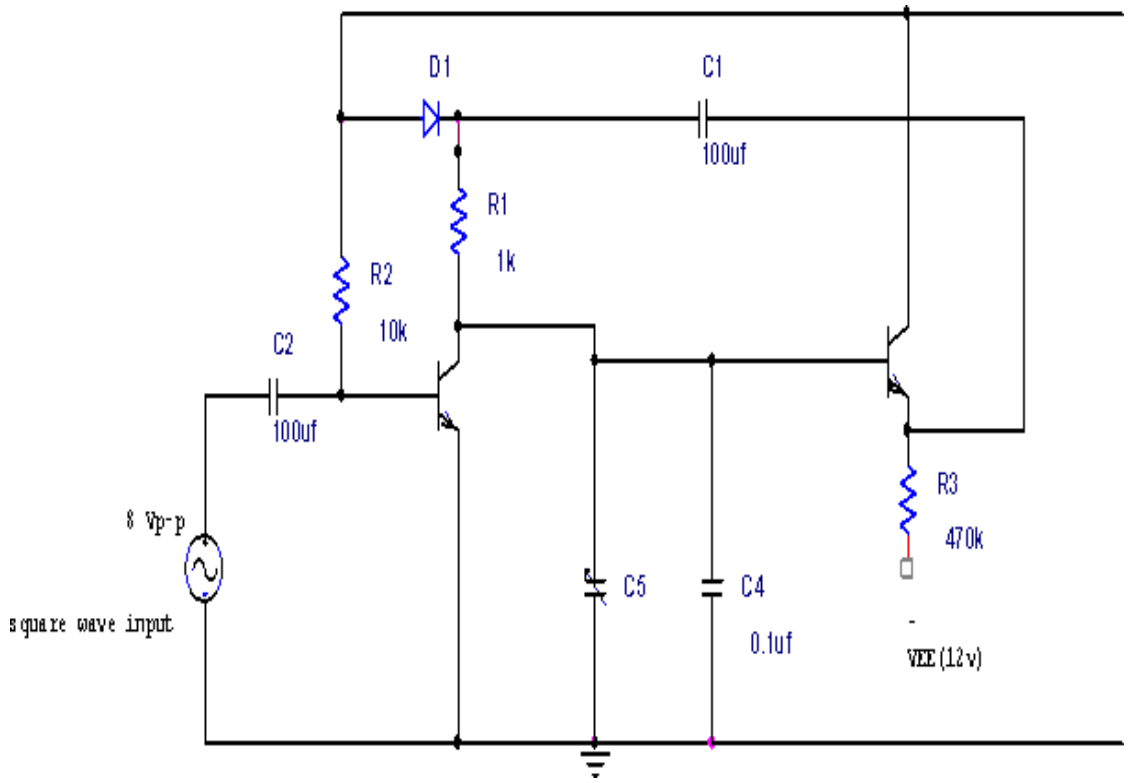
In this circuit both V & R are fixed magnitude current I is constant. This constant current I flowing through the capacitor develops a ramp voltage across it. Boot strap sweep circuit uses to generate a ramp voltage.

When the input V_i goes positive ,Q_1 off , potential of „A" rises. This increases of voltage at „A" is transmitted to „B" through Q_2 and capacitor C_B. The result is that the potential of „B" alsom rise by the same amount. This is the principle of Boot strap.

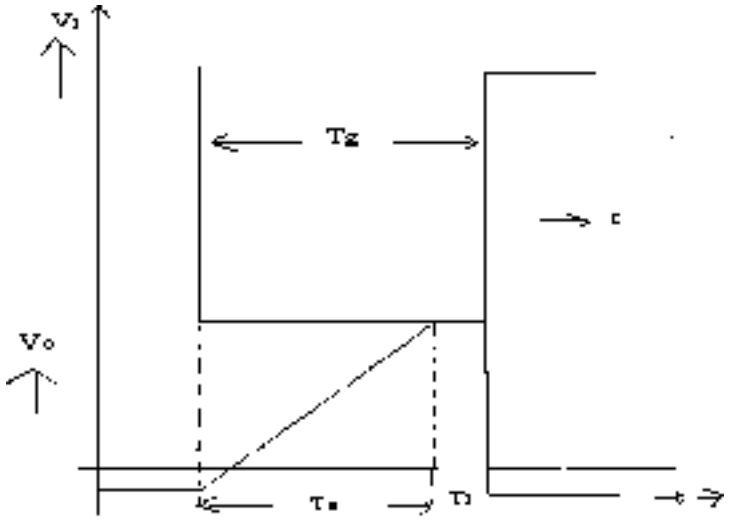
Procedure:

1. Connect the circuit as per the circuit diagram on bread board
2. Apply $8V_{PP}$ square wave input in function generator and V_{CC} = 12V & V_{EE} = -12V
3. Place the 300kpf from the decade capacitance box and note the output wave form across emitter of second transistor
4. Repeat the same by placing 400kpf & 500kpf in the place of variable capacitor
5. Plot the graph between V_i vs t & V_o vs

Circuit diagram:



Expected wave forms:



Result:

Thus the operation of Boot strap sweep generator is observe