FACULTY-PROFILE

Department: Electronics & Communication Engineering

1. Name : CH JAYAPRAKASH
2. Date of birth : 10TH MARCH 1983
3. Educational qualifications : : M.Tech,(Ph.D)
4. Area of specialization : VLSI
5. Date of joining : 14/05/2011
6. Designation : ASSISTANT PROFESSOR
7. Work experience
   - Teaching : 12
   - Research : 0
   - Industry : 0
   - Others : 0
8. Subjects teaching at
   - Under Graduate level : EDC,ECA,STLD,MP&MC,LICA,PDC,SS,VLSI,DICA,PDC,DLD
   - Post Graduate level : SMS,DSD
9. Projects guided at :
   - Under Graduate level : 9
   - Post Graduate level : 7
10. Professional bodies membership : ISTE,IETE
11. Postal Address : 17-2-84/1 LAKSHMI REDDI COLONY
    ASHOK NAGAR, JANGAREDDIGUDEM,
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14. Research Guidance : Masters / Ph.D : Masters
15. a) Projects carried out : --

    b) Patents : --

    c) Technology transfer : --

    d) Research Publications :

List of Journals :

S No	Author (s) Name	Title of the Research Paper	National/ International	Year of Publication	Name of the Journal	Vol.	Issue. No	Pages (PP)
1	Miranji Katta, R. Spandanalakshmi, M Narendra Kumar , Ch JayaPrakash	Static and Dynamic Analysis of CNT Cantilever for NEMS based Application.	International	Feb 2020	Journal of Computational and Theoretical Nanoscience (JCATN)	Vol:17	2	PP : 1-6
2	Miranji Katta, R, Ch JayaPrakash M Narendra Kumar ,vamsi krishna	Comparative analysis of lead-free piezoelectric material for ultrasonic glucose sensing applications	International	2019 APRIL	Jour of Adv Research in Dynamical & Control Systems, , , 2019	Vol. 11	02-Special Issue	1110-1116
3	Ch Jayaprakash	AREA & DELAY EFFICIENT DESIGN FOR PARALLEL PREFIX FINATE FIELD MULTIPLIER	International	OCT 2018	International Journal of Management, Technology And Engineering	Volume 8	10	2983-2988
4	Ch.Jaya Prakash Dr PHS Tejo murthy,Raji	Floating-point butterfly architecture based on redundant number system and Fused-Dot-Product-Add unit	International	2017	IJAERD(International Journal of Advance Engineering and Research Development)	4	11	60-66
5	CH JAYA PRAKASH M VISWESWARA RAO	A study on design and implementation of a real time embedded system for multiple image processing applications.	International	Aug 2016	IJRECE(Internation Journal Of Research In Electronics & Communication Engineering)	4	4	1550-1552
6	CH. JAYA PRAKASH U. APARNA DEVI,	An Efficient and Enhanced Low Power ETI Encoder for Serial Communication Links	International	2015	International journal of scientific engineering & technology Research (IJSETR)	4	10	1800-1804
7	CH JAYAPRAKASH K.N.U Maheswari	An advance4d & Low Power LBIST For Cryptographic Applications	International	2015	IRD India, International Journal on Advanced Computer Engineering and Communication Technology (IJACECT)	4	2	28-34
8	CH JAYAPRAKASH A MOHAN VAMSI KRISHNA	Design of low power scalable Digital Comparator using a parallel prefix tree	International	2014	International conference on electrical, electronics & computer systems(ICEECs)	2	8,9	24-27
9	CH JAYAPRAKASH, T.PrudhviRaju	Design of FIR Filter using Fifth approximation adder	International	2014	International journal technology Research in engineering (IJTRE)	3	2	124-127

10	CH. JAYAPRAKASH T. INDIRA	Design Of Low Power And High Performance Pulse Triggered Flip Flop Using Conditional Pulse Enhancement Method	International	2013	Interscience open access journal, International Journal of Electrical and Electronics Engineering (IJEEE)	3	2	25-31

e) No. of books Published with Details: --

16. Short term courses attended:

S No	Name of the workshop/ STTP	Place	Period	
			From	To
1	Mission10X workshop	Khammam	20/01/2009	24/01/2009
2	AICTE/MHRD summer School on Application of ICT for Hardware Laboratory	IIT KHARAGPUR	17/05/2009	23/05/2009
3	EMBEDDED SYSTEM PROGRAMMING(DEVICE DRIVERS) organized by CDAC Hyd in collaboration with JNTU H	CDAC HYD	18/05/2010	28/05/2010
4	Digital signal processing oraganiged by Dept of EEE Under QIP Programee	IIT ROORKEE UTTARAKHAND	26/02/2011	02/03/2011
5	Recent advancements in VLSI Technology & Design using EDA Tools conducted by CoreEL Technologies in collaboration with JNTUK	JNTU KAKINADA	20/07/2016	24/06/2016
6	One week training programmeon "INSTRUCTIONAL DESIGN AND DELIVERY SYSTEM"	SIR CRR COLLEGE OF ENGG	04/10/2017	9/10/2017

17. Organized/Delivered Seminars/Workshops/Guest lectures/FDPs/Refresher Courses:

S No	Name of the workshop/ STTP	Place	Period	
			From	To
1	One week workshop on "Advanced Vlsi Training On Xilinx FPGA Using Vivado Tools"	SIR CRREDDY COLLEGE OF ENGG, eluru	16/09/2019	21/09/2019
2	Guest lecture on real time application of signals n systems	SIR CRREDDY COLLEGE OF ENGG, eluru	6/09/2018	6/09/2018
3	Two day Workshop on "FPGA based system design using Verilog " during 6h & 7th October 2017	SIR CRREDDY COLLEGE OF ENGG, eluru	06/10/2017	07/10/2017
4	Two day Workshop on Two Day Work Shop On IC Design Flow Using Mentor Graphics Tools	SIR CRREDDY COLLEGE OF ENGG, eluru	05/08/2016	06/08/2016

18. Any Other
Achievements / Awards :

1. RATIFIED AS ASSISTANT PROFESSOR FROM JNTU HYD
2. RATIFIED AS ASSISTANT PROFESSOR FROM ANDHRA UNIVERSITY
3. RATIFIED AS ASSISTANT PROFESSOR FROM JNTUK

Ch. Jayaprakash

Date:

SIGNATURE