FACULTY-PROFILE

Department : Electronics & Communication Engineering

1. Name : HAREESH PANCHETI
2. Date of birth : 17th August 1987.
3. Educational qualifications : B.Tech, M.Tech,(Ph.D).
4. Area of specialization : VLSI Design.
5. Date of joining : 6th September 2010.
6. Designation : Asst.Professor.
7. Work experience
   - Teaching : 10 years 09 Months.
   - Research : 2 Years 6 Months
   - Industry : -NIL-
   - Others : -NIL-
8. Subjects teaching at
   - Under Graduate level : HST,PTRP,EMI,VLSID&ES,RENA,SS,DSP,MEFA,MS,SDTV,VLSI.
   - Post Graduate level : DSP,VLSID,VDT,VMDS,LPVD,CAICD,SoCD.
9. Professional bodies membership : AMIE, AMIETE, MIAENG.
10. Achievements / Awards :-NIL-
11. Postal Address : D.No: 7 / 244(A), Sri Venkateswara Nilyam, Sujatha Nagar 4th Lane, Ongole, Prakasam (D.T), Andhra Pradesh. PIN Code: 523002.
12. E-mail ID : hareeshpancheti@gmail.com
13. Mobile numbers : 903074461, 9618496159.
14. Research Guidance : **M.E / M.Tech – 11**

S.No.	A.Y	Title of the Project
1.	2011-2012	Adaptive Wiener Turbo Systems with JPEG & BIT Plane Compressions
2.	2012-2013	STDFF A Pass Transistor Based Flip Flop Design for Efficient Integrated Circuits
3.	2012-2013	A New Low Power Technology for Power Reduction in SRAM's Using Read Stability with Reduced Transistor Count for Future Catches
4.	2013-2014	Design Low-Power Pulse-Triggered Flip-Flop design based on a Signal Feed-Through Scheme
5.	2013-2014	A Digital CMOS Parallel Counter Architecture
6.	2014-2015	Low Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Using Power Gating Techniques
7.	2014-2015	Latency Optimized Square and Cube Architecture using Vedic Sutras
8	2015-2016	Design and implementation of Brent Kung carry select adder using pass transistor logic techniques
9	2015-2016	Hardware Implementation of Digital Watermarking System for Real Time Captured Image Transmitting
10	2016-2017	Design of DPLL and Implementation of BIST to Evaluate its characteristics
11	2017-2018	Delay analysis for current mode threshold logic gate Designs

B.E / B.Tech – 06

S.No.	A.Y	Title of the Project
1.	2011-2012	Embedded Pre-paid Energy meter using 89S52 Mico-Controler.
2.	2012-2013	PAPR Reduction of Space Frequency Block coded OFDM Systems Using Selected Mapping Algorithm without Side Information.
3.	2012-2013	Implementation of low power Digital FIR Filter Based on Low Power Multipliers and Adders.
4.	2013-2014	Advanced Sowing and Planting equipment controller Design using VHDL.
5.	2016-2017	GSM based Wireless Electronic Notice Board.
6.	2018-2019	Arduino based Gesture to speech conversion for the mute community.

15. a) Projects carried out : -NIL-
b) Patents : -NIL-
c) Technology transfer : -NIL-
d) Research Publications :
Conferences attended : 08 (National-02, Intrenational-06)

List of Papers presented in Conferences: 11(National-03, International-09)

S.No	Title of Paper	Conference		Date	Place
		National	International		
1.	A Novel Power Reduction Technology in SRAM's using Read Stability with Reduced Transistor Count for Future Caches for Low Power Applications		yes	29th September 2013	Chennai
2.	An Efficient Integrated Circuit Design For a Pass Transistor D Flip-Flop (STDFF)		yes	29th Sep-2013	Chennai
3.	MTCMOS Full Subtractor With Low Power Consumption and Reduced Leakage power	yes		24th & 25th January 2014	Eluru
4.	Exploiting Rising and Charge-Sharing Voltage for Power Management in High Speed Domino Circuits	yes		24th & 25th January 2014	Eluru
5.	Design Low-Power Pulse-Triggered Flip-Flop design based on a Signal Feed-Through Scheme		yes	12th October 2014	Coimbatore
6.	A Digital CMOS Parallel Counter Architecture		yes	12th October 2014	Coimbatore
7.	Latency optimized square and Cube Architecture using Vedic Sutras		yes	April 2015	Hyderabad
8.	Low Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Using Power Gating Techniques		yes	10th May 2015	Guntur
9.	Design and implementation of Brent Kung carry select adder using pass transistor logic techniques		yes	16th September 21016	New Delhi
10.	Hardware Implementation of Digital Watermarking System for Real Time Captured Image Transmitting		yes	05th November 2016	New Delhi
11.	Constant Threshold logic gates Design	yes		12th &13th November 2018	Annamalai University, Chidambaram

List of Journals: 14 (National-0,International-14)

S.No	Title of paper (Authors)	Journal		Name of the Journal in which paper is published	Impact factor, volume number, Issue number, Page number, Year ISSN Number
		National	International		
1.	K. Hari Krishna, P. Hareesh, "A New Low Power Technology for Power Reduction in SRAM's Using Read Stability with Reduced Transistor Count for Future Catches"		yes	IJESS	Vol-3,pp. 88-91, ISS-2,2013,ISSN:2231-5969.

2.	G. Lakshmi Praeetha, P. Hareesh "STDFF A Pass Transistor Based Flip-Flop Design for Efficient Integrated Circuits"		yes	IJESS	Vol-3, pp. 114-117, ISS-2, 2013, ISSN: 2231-5969.
3.	P.Hareesh, K. Harikrishna, G. Lakshmi Praneetha, "MTCMOS Full Subtractor With Low Power Consumption and Reduced Leakage power"		yes	IJECT	IMPACT Factor: 1.319 (2015) International Scientific Indexing. Vol.5, pp.71-73, Issue Spl-3, Jan-March 2014, ISSN: 2230-7109(Online), ISSN: 2230-9543(Print).
4.	P. Hareesh, R.Trinadh, V.Krishnan,G.N.Murthy, "Exploiting Rising and Charge-Sharing Voltage for Power Management in High Speed Domino Circuits",		yes	IJECT	IMPACT Factor: 1.319 (2015) International Scientific Indexing. Vol.5, pp.77-80, Issue Spl-3, Jan-March 2014, ISSN: 2230-7109(Online), ISSN: 2230-9543(Print).
5.	M.Greeshma, P.Hareesh,"Design Low-Power Pulse-Triggered Flip-Flop design based on a Signal Feed-Through Scheme"		yes	IJEECS	IMPACT Factor: 2.04 Vol.2, pp.28-31, Issue-8, 9, 2014, ISSN: 2347-2820(Online).
6.	Anupama.Ch, P.Hareesh, "A Digital CMOS Parallel Counter Architecture",		yes	IJEECS	IMPACT Factor: 2.04 Vol.2, pp.38-42, Issue-8, 9 2014, ISSN: 2347-2820(Online).
7.	Sk.Abdual Kadar, P.Hareesh, "Low Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Using Power Gating Techniques",		yes	IJMETMR	IMPACT Factor: 1.7450 (2015) International Journal Impact Factor. ISSN No: 2320-3706(Print) ISSN No: 2348-4845(Online).
8.	Ch.Salini, P.Hareesh, "Latency Optimized Square and Cube Architecture using Vedic Sutras"		yes	IJSETR	IMPACT Factor: 4.162 Vol.04, Issue No.19, June-2015, ISSN 2319-8885.
9.	P.Venkatesh,P. Hareesh,'' Hardware Implementation of Digital Watermarking System for Real Time Captured Image Transmitting''		yes	IJITECH	IMPACT Factor: 3.864 ISSN 2321-8665 Vol.04,Issue.10, August-2016, Pages:1733-1736
10.	A. Suresh Babu, P. Hareesh "Design and implementation of Brent Kung carry select adder using pass transistor logic techniques"		yes	IJRECE	Vol–4, Issue-3. Mar - Apr, 2016, ISSN:2321-5593(Online) ISSN: 2321-032X(Print)
11	P.Hareesh, S V Abhishek "Design of DPLL and Implementation of BIST to Evaluate its Characteristics"		yes	IJAERD (UGC Approved)	Vol-04,issue 11, November -2017, e-ISSN: 2348-4470, p-ISSN: 2348-6406

12	P.Gopi Krishna,K.Srinivasa R P.Hareesh,D.Ajay Kumar H.Sudhakar." Implementation of Bi-Directional Blue-Fi Gateway in IoT Envoriment"		yes	IJET (Scopus)	Vol-07, Special issue 8,2018,pages-97-102 ISSN: 2227-524X
13	P.Hareesh,Ch Jaya Prakesh, P Geetha "Concede Threshold Analysis for logic gate Designs"		yes	IJMTE (UGC Approved)	Vol-8,Issuse-X,October-2018, Pages-1861-1867, ISSN:2249-7455
14	Ch Jaya Prakesh, P.Hareesh, Sk. Farishma "Area and delay efficient design for parallel Prefix finite field multiplier"		yes	IJMTE (UGC Approved)	Vol-8,Issuse-X,October-2018, Pages-2983-2988 ISSN:2249-7455

e) No. of books Published with Details: -NIL-

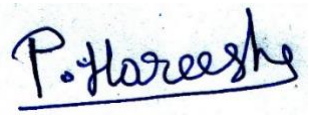
16. Short term courses attended: 09

S.No	Seminars/Workshops /Guest/lectures/FDPs/ Refresher Courses/NPTEL	Title	Organization/ Institution	Date
1.	Three day's national level Workshop	"Analog & Digital VLSI Circuits Design" using Cadence EDA Tools	Dept. of E.C.E, ACE Engineering College, Ankushapur(V), Gatkesar(M), R.R. Dist., A.P, India.	Dated 27th to 29th June, 2011
2.	One day Workshop	"Analog, Digital and Mixed Signal VLSI Design",	Dept. of E.C.E, Gudlavalleru Engineering College, Seshadri Rao Knowledge Village, Gudlavalleru, Krishna Dist., A.P, India	Dated 15th October, 2011.
3.	A two day's Workshop	"VLSI Design"	School of Electronics, Vignan University, Vadlamudi, Guntur Dist., A.P, India.	Dated 6th to 7th February, 2012.
4.	One day Workshop	"PLC Programming & Applications"	Sir C R Reddy College of Engineering, Eluru, W.G (D.T),A.P,India.	Dated 1st March 2015
5.	Five day's Workshop	"Recent Advancements in VLSI Technology and Design Using EDA Tools(VLSITP-2016)"	JNTU,UCOEK(A), Kakinada,A.P,India.	Dated 20th -24th July, 2016.
6.	Two day's Workshop	"IC Design Flow using Mentor Graphics EDA tools"	Sir C R Reddy College of Engineering,Eluru, W.G(D.T),A.P,India.	Dated 5th & 6th August 2016
7.	Two day's Workshop	"3D Modelling of Electromagnatic Systems Using ANSYS RF-Tools"	Sir C R Reddy College of Engineering,Eluru, W.G(D.T),A.P,India.	Dated 9th &10th September 2016.
8.	Two day's Workshop	"FPGA based system design using Verilog"	Sir C R Reddy College of Engineering,Eluru, W.G(D.T),A.P,India.	Dated 6th &7th October 2017.
9.	One week **FDP**	"CMOS Analog IC Design"	V R Siddharth Engineering College,Vijayawada, Krishna(D.T),A.P., India.	13th -18th November 2017.
10	NPTEL(8 weeks) - One Week	"Introduction to Research"	NPTEL-IITM	

17. Organized/Delivered Seminars/Workshops/Guest lectures/FDPs/Refresher Courses:

S.No	Seminars/Workshops/Guest lectures/FDPs/Refresher Courses	Title	Organization/Institution	Date
-NIL-				

18. Any Other : -NIL-



Date: 23-06-2021 SIGNATURE