FACULTY-PROFILE

Department: Electronics & Communication Engineering

1. Name : Trinadh Rajanala
2. Date of birth : 12th March 1988
3. Educational qualifications : M.Tech
4. Area of specialization : Embedded Systems
5. Date of joining : 27-08-2012
6. Designation : Assistant Professor
7. Work experience
   - Teaching : 09 Years
   - Research : -
   - Industry : -
   - Others : -
8. Subjects teaching at
   - Under Graduate level : VLSI & Embedded Systems, Computer Networks, Data Communications
   - Post Graduate level : Wireless Communications, Cellular & Mobile Communications, VLSI Design
9. Projects guided at :
   - Under Graduate level : 08
   - Post Graduate level : 04
10. Professional bodies membership : AMIE: AM163850-8, IAENG – 134035
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13. Research Guidance : Masters / Ph.D : Masters

S.No.	Title of the project
1.	Design and Area Optimization of 1KB Memory using 45nm CMOS 6T SRAM Cell
2.	Folded Architecture based Carry Skip Adder for M-Bit
3.	A low power new data compression algorithm for wire/wireless sensor network using K-RLE
4.	A design of area and power efficient high-speed data path logic system.

15.Research Publications :

List of Conferences:

S.No	Title of paper	Conference		Date	Place
		National	International		
1.	A novel design of area and power efficient high speed data path logic system.	-	International Conference on Systemics, Cybernetics and Informatics	July, 2014	Hyderabad
2.	Enhanced feature sets for face recognition under difficult lighting conditions.	-	International Conference on Nanoscience Engineering & Advanced computing	July 8-10, 2011	Narasapuram

List of Journals:

S.No	Title of paper (Authors)	Journal		Name of the Journal in which paper is published	Impact factor,volume number,Issue number Page number,Year ISSN Number
		National	International		
1.	Design and Area Optimization of 1KB Memory using 45nm CMOS 6T SRAM Cell	-	Yes	IJAEMA	Vol. 12, Issue – 7, Pg: 2120-2125, July – 2020, ISSN NO:0886-9367
2.	Folded Architecture based Carry Skip Adder for M-Bit	Yes	-	JETIR	Impact Factor: 5.87, Vol. 5, Issue -12, Pg: 128-133, December 2018, ISSN: 2349-5162
3.	Design and development of smart energy meter for	-	Yes	IJET	Scopus Indexed Vol. 7, Slp Issue -2.8, Pg: 115-

	effective use of electricity in IoT applications				119, March 2018, ISSN: 2227-524X
4.	Exploiting rising and charge sharing voltage for power management high speed domino circuits.	-	Yes	IJECT	Impact Factor: 0.675, Vol. 5, Issue spl -3, Pg: 77-80, March 2014, ISSN: 2230-7109 (online), ISSN: 2230-9543
5.	A design of area and power efficient high speed data path logic system.	-	Yes	IJEEE	Impact Factor: 0.501, Vol – 3, Issue – 2, Pg: 50-55, 2013, ISSN: 2231-528.
6.	A low power new data compression algorithm for wire/wireless sensor network using K-RLE.	-	Yes	IJESS	Impact Factor: 0.501, Vol -3, Issue – 2, Pg: 81-87, 2013, ISSN: 2231-5969.
7.	Architecture for adaptive rood pattern search algorithm for motion estimation.	-	Yes	IJERT	Impact Factor: 0.898, Vol – 1, Issue – 7, Pg: 1-5, Sept – 2012, ISSN: 2278-0181.

Date: 22-06-2021 SIGNATURE