Ref. No: SIRCRRCE/ECE/BOS/2025-26/470   Date: 04-12-2025

To
The Principal,
Sir C Reddy College of Engineering,
Eluru

Subject: Request for Approval to Conduct BOS Meeting for M.Tech CR25 Course Structure

Respected Sir,

   With reference to the academic requirements for framing the **M.Tech CR25 Course Structure**, we hereby request your approval to conduct the **Board of Studies (BOS) Meeting**. The purpose of this meeting is to finalize the course structure as per CR25 guidelines, incorporate industry-relevant updates, and ensure compliance with university and regulatory standards.
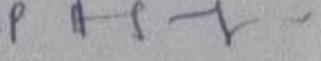
The BOS meeting is scheduled as follows:

- **Date:** 06-12-2025
- **Mode:** Online (Zoom Meeting)
- **Time:** 10:00 AM to 12:00 Noon

   We kindly request you to approve the conduct of the meeting and permit us to proceed with sending invitations to the BOS members.

Thanking you sir,
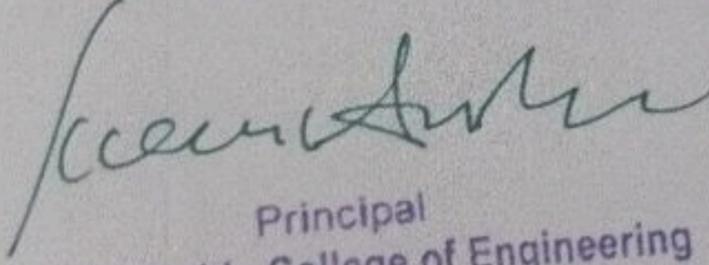
Principal
Sir C R Reddy College of Engineering
ELURU - 534 007

(Dr. P H S Tejo Murthy)
HOD-ECE
Head of the Department
Electronics & Communication Engg.
Sir C.R.R.College of Engineering
Eluru - 534 007

3rd BOS Meeting

Dt:- 6-12-2025

Minutes of BOS meeting M.Tech, VLSI (A.Y: 2025-26).

Subject:- M.Tech, VLSI, CR-25 course structure & syllabus.

Date:- 06/12/25.

Venue:- Department office of E.C.E.

Time:- 10:00 A.M to 12:00 P.M.

Mode of conducting meeting:- online meeting through Zoom app.

Agenda:-

(i) Introduction to BOS members.

(ii) To discuss and finalize the proposed Ist year & IInd year M.Tech Ist sem to IIIrd sem M.Tech, VLSI course of CR-25 Regulations.
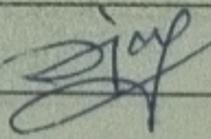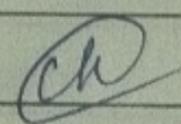
(iii) Finalization of model paper and list of paper setters.

(iv) To finalize the evaluation procedure for Continuous internal evaluation (CIE) and Semester end evaluation (SEE

(V) Ratification of course objectives and course outcomes, CO-PO mapping for the proposed subjects.

(vi) Finalization of Textbooks and Reference Books.

(vii) Any other item with the permission of the chairman

Board of members details :- 3rd BOS meeting.

S.No	Name of the Members	Designation	Designation in committee.	Status of attending & signature.
1.	Dr. P.H.S. Tejo Murthy.	Prof. & HOD of Sir C.R.R.C.O.E.	Chair person.	P 4
2.	Dr. N. Balaji.	Professor & HOD JNTU, Kakinada	Member. university Nominee & Subject Expert.	online
3.	Dr. P. Sreehari Rao.	Professor, NIT, Warangal	Member (subject Expert)	online
4.	Dr. Puli Kishore.	Professor, NIT T.P. Gudem.	Member (Subject Expert)	online
5.	Dr. K. Murali Krishna	HOD, Mechatronics MSME.	Member (Industrial Expert)	online
6.	Dr. Chilaka Mahesh.	Director, Airport authority of india.	Member (Alumni)	Absent
7.	Dr. M. Ravi Kumar.	Professor Sir CRRCOE.	Member.	
8.	Dr. D. Ajay Kumar.	Asso. Professor Sir CRRCOE.	Member (M.Tech, Coordinator)	Ajay
9.	Dr. ch. Jaya Prakash	Asso. Professor Sir CRRCOE.	Member	Ch
10.	Dr. K. Radha.	Asso. Professor. Sir CRRCOE.	Member	Super

Discussion & finalization of CR-25 (M. Tech. VLSI) Syllabus and course structure :-

(i) Digital CMOS circuit design :- Member of subject expert Dr. P. Sreehari Rao garu suggested text book Jan Rabaey, Anantha Chadrakasan, B. Nikolic "Digital integrated circuits : A design Perpective", prentice Hall of india, 2nd edition, Feb 2003.

(ii) Anlog CMOS circuit design :- Member of university nominee Dr. N. Balaji garu suggested textbook of "Design of Analog CMOS integrated circuits, Behzad Razavi, TMH edition".

(iii) MOS Device physics :- Suggested Text books of "Dasgupta, Nandita, Dasgupta Amitava - SemiConductor Devices : Modeling and Technology, PHI - learning Pvt. Ltd 2004, and Yannis Tsivdis, colin McAndrew. "operation and Modeling of MOS Transistor" oxford university press, 2011 by the member of subject expert Dr. P. Sreehari Rao garu.

(iv) VLSI Technology :- Dr. Sreehari Rao garu and Dr. N. Balaji garu suggested text book of S.M Sze, "VLSI Technology", Tata Mcgraw-Hill, second edition, 2017. as a Reference.

(v) Digital system design through HDL :- Member of Subject expert Dr. P. Suggested textbook of Stephen Brown & Zvonko Voranesic, Fudamental of digital logic design with VHDL, Tata Mcglaw-Hill.

(vi) Low Power VLSI design :- low Power CMOS VLSI Circuit design Kaushik Roy, Sharat C. Prasad, wiley india Pvt. limited, feb. 2 2009 Suggested by Dr. P. Sreehari and N. Balaji garu.

(vii) Analog CMOS circuit design Lab :- Dr. P. Sreehari Rao garu Suggested experiments 10th & 11th may removed and keep in mixed signal circuits design lab and suggested to add the name of the experiments are :

Bandgap reference (BGR), design of memories and to integrate lab experiments. Morning section - theory and afternoon section see conducted lab. Need to conduct eight weeks - hands on session. Suggested candence tool.

(viii) Digital CMOS circuit design - Dr. P. Sreehari Rao garu. Dr. N. Balaji garu suggested experiments design ALU circuit and find out power dissipation and propagation delay. Do simple experiments pseudo logic and findout Power dissipation and propagation delay.

(ix) CMOS Mixed Signal circuit design - Dr. Sreehari Rao garu suggested text book of Behzad Razavi "RF Micro electronics" prentice Hall of india, 2001.

(X) CMOS Mixed signal circuit design lab :- Need to add 10th & 11th experiments from CMOS analog IC design lab experiments and also add high speed and high gain comparators suggested by Dr. P. Sreehari Rao garu and Dr. N. Balaji garu.

(xi) Quantum Computing :- All the board of members i.e, Dr. N. Balaji garu. Dr P. Sreehari Rao garu. Dr. Kishore garu and Dr. K. Murali Krishna Suggested AI/ML based subject to be added as a elective. so, Quantum computing suggested as a elective in 2nd semester.

(xii) Research Methodology & IPR:- Government Support to Technology transfer to be added in this subject.

(xiii) Internship / Industrial Training :- Dr. K.Murali Krishna garu. Industrial expert suggested industrial Automation to be added as an elective.

Resolution :-

All the above suggestions and modifications were discussed and approved by BOS members. The concerned faculty members are requested to incorporate the approved changes in the syllabus and revised documents to final approval.

Estd.1989

SIRCRREDDYCOLLEGEOFENGINEERING
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(SPONSOREDBYSIRCRREDUCATIONALINSTITUTIONS,SOCIETYREGD.NO.10/1958)
VATLURU, ELURU-534007, ELURUDISTRICT, ANDHRAPRADESH, INDIA
Approved by AICTE, Accredited By NBA (UG: CSE, IT, ECE, EEE, ME), Affiliated To JNTUK, Kakinada

Minutes of BOS Meeting M.Tech ,VLSI (A.Y:2025-26)

3rd BoS Meeting

Subject: M.Tech (VLSI) 1st Year 1st – IIIrd Semester (Theory and Labs).

Date: 06/12/2025

Venue: Department Office of ECE.

Date & Time: 06-12-2024, 10:00 A.M.

Mode of conducting meeting: Online meeting (Zoom App).

Agenda:

1. Introduction of BOS members
2. To discuss and finalize the proposed 1st Year M. Tech. 1st – IIIrd Semester VLSI Design (Theory and Lab) courses of CR -25 regulations.
3. Finalization of Model Paper and List of Paper Setters.
4. To finalize the evaluation procedure for continuous internal evaluation (CIE) and semester end evaluation (SEE)
5. Ratification of Course Objectives and Course Outcomes, CO–PO Mapping for the proposed subjects.
6. Finalization of Text Books and Reference Books.
7. Any other item with the permission of the chairman.

Board of Members details:

S.NO	Name of the Member(s)	Designation	Designation in Committee	Status attending	Signature
1	Dr. P.H.S.TejoMurthy	Professor & HOD, SIRCRRCOE	Chairperson	In Person Details	PH
2	Dr. N. Balaji.	Professor & HOD, JNTU, Kakinada	Member (University Nominee)	NB online	NB
3	Dr. Puli Kishore Kumar	Professor, NIT, T.P.Gudem	Member (Subject Expert)	← online →	
4	Dr.P.Sreehari Rao,	Professor, NIT, Warangal.	Member (Subject Expert)	← online →	
5.	Dr. Murali Krishna	HOD, Mechatronics MSME,	Member (Industrial Expert)	← online →	
6.	Dr. Chilaka Mahesh	Director, Airport Authority of India	Member (College Alumni)	← online →	
7.	Dr. M. Ravi Kumar	Professor, SIRCRRCOE	Member	In person	M

8.	Dr. D. Ajay Kumar	M.tech Coordinator SIRCRRCOE	Member	In Pers—	217
9.	Dr. Ch. Jaya Prakash	Assoc.Professor, SIRCRRCOE	Member	In Person.	Ch
10.	Dr.K.Radha	Asst.Professor, SIRCRRCOE	Member	Inperson	Radhy.

Discussion & Finalization of Syllabus of M.Tech ,VLSI (CR-25)

Digital CMOS Analog IC Design: Member of University nominee Dr.N.Balaji garu suggested Design of Analog CMOS Integrated Circuits — Behzad Razavi, TMH Edition.

Digital CMOS Circuit Design : Member of subject expert Dr.P.Sreehari Rao garu suggested Jan Rabaey, Anantha Chandrakasan, B Nikolic," Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003text book referred in digital CMOS Circuit design.

MOS Device Physics: Suggested Text books on "Dasgupta Nandita , Dasgupta Amitava ,Semiconductor Devices: Modelling And Technology, PHI learning Pvt.Ltd,2004 and Yannis Tsividis, Colin McAndrew "Operation and Modeling of the MOS Transistor" Oxford University Press, 2011 by Dr.P.Sree Hari Rao garu.

VLSI Technology: Dr.P.Sree Hari Rao garu Suggested textbook of S.M. Sze, "VLSI technology, Tata McGraw-Hill, Second Edition" , 2017. as Reference .

Digital System design through HDL : Member of subject expert Dr. Puli Kishore Kumar garu suggested text book Stephen Brown & Zvonko Vranesic, Fundamentals of Digital Logic Design with VHDL, Tata McGraw Hill, 2nd edition.

Low Power VLSI Design : Suggested text book "Low-Power CMOS VLSI Circuit Design. Kaushik Roy, Sharat C. Prasad. Wiley India Pvt. Limited, Feb 2, 2009" by Dr.P.Sreehari Rao garu and Dr.Balaji garu.

Analog CMOS Circuit Design Lab: Dr.P.Sreehari Rao garu suggested Experiments 10th and 11th may be removed and keep in mixed signal circuit design lab and also suggested to add the name of the experiments are: Bandgap references (BGR), design of memories and to integrate lab experiments. Morning section –theory and afternoon section: Lab. Need to conduct eight weeks- hands on session. Suggested cadence software.

Digital CMOS Circuit Design Lab: Dr.P.Sree Hari Rao garu suggested Experiments deign ALU Circuit and find out Power dissipation and Propagation delay. Deign simple experiment pseudo logic and find out Power dissipation and Propagation delay.

CMOS Mixed Signal circuit Design: : Dr.P.Sreehari Rao garu suggested text book Behzad Razavi, "RF Microelectronics Prentice Hall of India,2001 .

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CMOS Mixed Signal circuit Design Lab: Need to add 10th &11th experiments from CMOS analog IC design Lab experiments and also add high speed & high gain comparators suggested by Dr.P.Sreehari Rao garu and Dr.N.Balaji garu.

Quantum Computing: All the BOS members are suggested AI/ML-based subject to be added as an elective. Quantum computing subject to be added as an elective.

Research Methodology and IPR: To add government support for technology transfer in the 5th unit suggested by Dr. Puli Kishore Kumar.

Summer Internship/ Industrial Training : Dr. Murali Krishna garu. Industrial Expert proposed Industry Automation to be added as an elective.
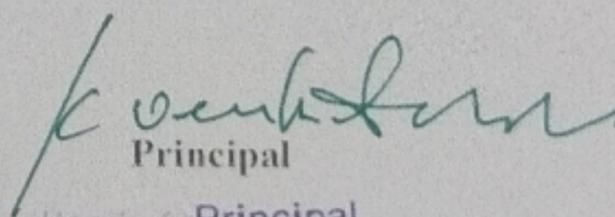
Resolution

All the above suggestions and modifications were discussed and approved by the BOS members. The concerned faculty members are requested to incorporate the approved changes in the syllabus and submit the revised documents for final approval.
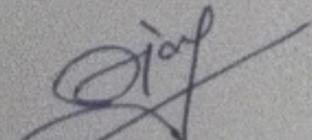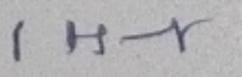
M.Tech Coordinator   **HOD-ECE**   Principal

Head of the Department
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