Code No: R1621042 **R16** SET - 1

II B. Tech I Semester Supplementary Examinations, October/November - 2020
SWITCHING THEORY AND LOGIC DESIGN
(Com to ECE, EIE and ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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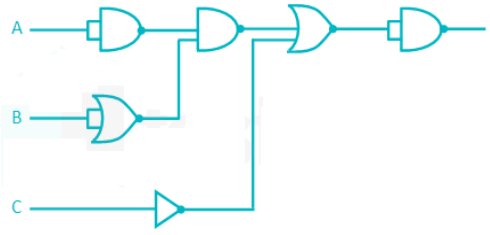
PART –A

1. a) Express decimal digits 0-9 in BCD code and 2 4 2 1 code. (2M)

   b) Implement the function F(x , y , z) = ∑(0 , 6) with NAND gates. (3M)

   c) For the figure given, the output will be. (3M)



   d) Explain basic structure of PAL. (2M)

   e) Convert JK Flip Flop to D Flip Flop. (2M)

   f) Explain the representation of State Diagram in detail. (2M)

PART -B

2. a) What is a reflected code? Write about reflected codes by giving examples. (7M)

   b) Design BCD code to Gray code converter. (7M)

3. a) Obtain the simplified expressions in sum of products for the following Boolean functions using Karnaugh-Map. (7M)
   i) F(A, B,C,D) = Σ (7,13, 14, 15) ii) F(w,x,y,z) = Σ (2,3,12,13,14,15)

   b) Minimize the following Boolean expressions to the required no. of literals (7M)
   i) BC + AC'+AB+BCD to four literals
   ii) ABC+A'B'C +A'BC+ABC'+A'B'C' to five literals

4. a) Derive Boolean expression for a 2input Ex-OR gate to realize with 2 input NAND gates without using complemented variables and draw the circuit. (7M)

   b) Redraw the given circuit in (figure4)after simplification. (7M)

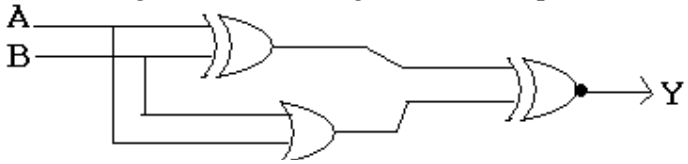


Figure 4

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5. a) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit. (7M)

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

   b) Derive the PLA programming table for the combinational circuit that squares a 3 bit number. (7M)

6. a) What is flip-flop? How can be used in sequential circuit and explain in detail. (7M)

   b) Explain about Master-slave flip-flop in detail. (7M)

7. a) The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x2 changes from 0 to 1 while x1=1. The output changes from 1 to 0 only when x1 changes from 1 to 0 while x2=1. Find a minimum row reduced flow table. (7M)

   b) Draw the state diagrams of a sequence detector which can detect 101. (7M)